



GP3 Gigabit Speed Embedded Computer

ODM Reference Board for Motorola PowerQUICC III

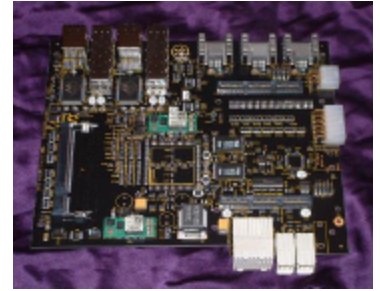


**RIO HIP
Compliant!**

**Dual Gigabit Ethernet (both copper and fiber)
8 bit Parallel RIO (Rapid IO) and PC104plus 32bit PCI
Local Bus Expansion (FPGA option card for protocol/ASIC design Q2)**

Motorola PowerQUICC III CPU Chip Features

e500 Book E compatible core available from 800 MHz up to 1.5 GHz
32-bit, dual-issue, superscalar, seven-stage pipeline
32 KB L1 data and 32 KB L1 instruction cache (MMUs)
256 KB on-chip L2 cache with direct mapped capability
SIMD extension with single precision floating point
High-performance RISC CPM; 1 Gbps aggregate bandwidth
Two UTOPIA Level II master/slave ports with multi-PHY support
Eight TDM interfaces (T1/E1), two TDM ports that can be interfaced with T3/E3
ATM transmission convergence layer (8 channels) and inverse multiplexing (IMA)
MII, Serial, and various other CPM comm. ports offloaded from the e500 core
Integrated high-performance security processor function (optional by CPU)



Software

Integral OS-less monitor diagnostic preloaded in flash
2.4.26 GPL embedded Linux kernel preloaded in flash



boot in seconds, start development in minutes!

Please check out our software partners!

GPL Linux and Integration Services- www.embeddededge.com
QNX Neutrino- with true SMP in the Momentics IDE www.QNX.com
OSE- the ultra-reliable message passing solution www.OSE.com
Abatron BDI2000- on chip debugger- www.ultsol.com

Ask us about your military DO-178B certification requirements

GP3 Product Description

Board Size

6.75x8.00 Inches
EBX compatible mechanical mounting
holes plus 1/2 inch on each side for RIO

Operating Temperature

Standard version 0 to 40deg C
Extended temperature TBD

Weight

375g

Power Requirement

60Watt compact wall supply included

An exceptionally powerful single board computer/router designed as both a stand-alone product, as well as for reference board and custom integration purposes. The Motorola book "E" core allows for stateful packet inspection and manipulation as well as policy/QoS enforcement. Integrated MACs for the the TSEC (triple speed Ethernet controllers) give customers granular and deterministic control over data flow- a critical feature in the medical, military, network/telecom, test & measurement, and industrial control markets.

Price is approx 500\$ in qty 1k

Ordering information

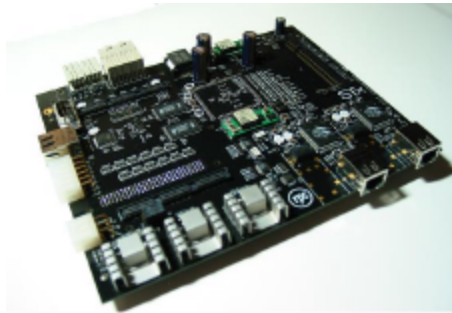
GP3-8560 (for MPC8560)-xxxx
GP3-8555 (for MPC8555)-xxxx
GP3-8540 (for MPC8540)-xxxx
GP3-8541 (for MPC8541)-xxxx

Last 4 digits are
CPU clock speed
In Megahertz

With every board you get: wall power supply, cable kit (Serial, PCI Power, Enet both standard and reverse), warranty card, PDF schematic, and software resource CD.

Accessories

Base configuration is 1 bank of 256 mbyte DDR memory [GP3DIMM0256](#)
memory modules from 256 mbyte to 2048 mbytes (2 gbytes) [GP3DIMM-xxxx](#) each available
single or multimode [GP3SFP-xx](#) (specify km for single mode) fiber gigabit Ethernet module
The GP3 supports up to 4 gigabytes of DRAM



Capabilities

- Stateful packet management
- IP and ATM internetworking
- QoS and policy enforcement
- Real-time gigabit data flow

Applications and Markets

- Security Appliances
- Ultra Highspeed Radio A.P.
- VOIP/Telecom Gateway
- Gigabit Test & Measurement
- Industrial or Network Router

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Coming in Q3 2004, the G3Pio card!

Plugs onto the PowerQUICC III local bus (expansion card)
Has a XILINX Virtex II FPGA/Pro for protocol/ASIC development,
RapidIO testing or data-plane acceleration



G3Pio Features

XILINX Virtex II FPGA/Pro
Xilinx CPLD for full configuration of
interface to PowerQUICC 3
Jedec 80pin Flash module
Dual ZBT local SRAM
Independent Power supply & cooling



*GP3 is an acronym
for the Gigabit
Packet Processor
Project*