

Silicon Turnkey eXpress

Embedded Engineering Solutions

Serial RapidIO Development Platform for the Tundra Semiconductor Tsi568A Hardware Manual



Silicon Turnkey Express
749 Miner Road • Highland Heights, Ohio 44143
Phone (440) 461-4700 • (800) 827-2650

©Copyright 2006, Silicon Turnkey Express
A division of RPC Electronics Inc., All Rights Reserved.

Revision History

Rev	Date	Comments
A	Jan, 2006	Initial release of manual
B	Sep, 2006	Revised format
C	Oct, 2006	Revise Figure 1 and naming on various tables
D	Nov. 27, 2006	Revised table SW5
E	Dec. 4, 2006	Added notes to sections 1.2.10, 1.2.12, 2.3.1.1, 2.3.1.2, 2.3.3 and 3.1

NOTICE

The information contained within this guide is the property of Silicon Turnkey Express, and except as otherwise indicated shall not be reproduced in whole or in part without the explicit written authorization of STx. The distribution of this document outside of the company is prohibited without the written authorization of STx.

The following information is intended to alert the user to possible dangers and important information contained within this guide. The **“WARNINGS”**, **“CAUTIONS”** and **“NOTES”** do not eliminate these dangers. Close attention to the information supplied along with “common sense” operation is the major accident prevention measure.

WARNING:	Failure to follow this warning may result in bodily injury.
-----------------	---

CAUTION:	Failure to follow this caution may result in possible damage to the board.
-----------------	--

NOTE:	Failure to follow this note may result in improper results from the board.
--------------	--

Table of Contents

1.0	GENERAL DESCRIPTION.....	6
1.1	Device Placement	6
1.2	Power Connectors.....	7
1.2.1	J43 – ATX Input Power Connector.....	7
1.2.2	J36 and J37 – Auxiliary Output Power Connectors.....	8
1.2.3	JP2 – PSON/Power Enable Jumper (ATX Power Enable).....	8
1.2.4	System Reset Switch SW1.....	8
1.2.5	SMA Connector Port Allocation.....	8
1.2.5.1	Serial Port 0.....	8
1.2.5.2	Serial Port 8.....	9
1.2.6	J42 - Infiniband Port Allocation.....	10
1.2.7	J33 - Serial RIO Interface Port Allocation.....	10
1.2.8	J34 – Power.....	11
1.2.9	J35 - Power	11
1.2.10	Configuration/Programming.....	11
1.2.10.1	SW2 – Power Down Configuration Dipswitch	12
1.2.10.2	SW4 – Power Down Configuration Dipswitch	13
1.2.11	SW3 – Mode Select Programming Dipswitch.....	14
1.2.12	SW5 – Speed Configuration Dipswitch.....	15
1.2.13	J44 – External Control Port	16
1.2.14	JTAG Headers.....	25
1.2.14.1	J45 - Tsi568A JTAG Header	25
1.2.14.2	J46 - AMC JTAG Header	25
1.2.15	J38 - External Status Port.....	26
2.0	SRDP HARDWARE DESIGN & ARCHITECTURE	27
2.1	General Description.....	27
2.2	Physical Specifications.....	27
2.3	Hardware Configuration	28
2.3.1	Clocking and Port Speed.....	28
2.3.1.1	S_CLK1	29
2.3.1.2	S_CLK2	29
2.3.2	Port Speed Selection – SW5.....	30
2.3.3	I ² C External EEPROM Enable Jumper – JP1.....	31
2.3.3.1	I ² C Interface.....	31
2.4	Logic Analyzer Test Connectors (J47 to J52)	31
3.0	SRDP CONNECTIVITY & CONFIGURATION.....	33
3.1	Default Settings	33
	Appendix A – Schematics	34

Table of Figures

Figure 1 – SRDP Card Top View	6
Figure 2 -- SRDP Card Bottom View.....	7
Figure 3 – Block Diagram.....	27

1.0 GENERAL DESCRIPTION

The Serial RapidIO Development Platform (SRDP) is a standalone evaluation platform for Tundra Semiconductor's Tsi568A 8-port Serial RapidIO Switch.

1.1 Device Placement

This section will provide a general description of the main components, connectors and switches associated with the Serial RapidIO Development Platform (SRDP).

Figure 1 below is an overall top view of the SRDP board and shows locations of the key components and connectors.

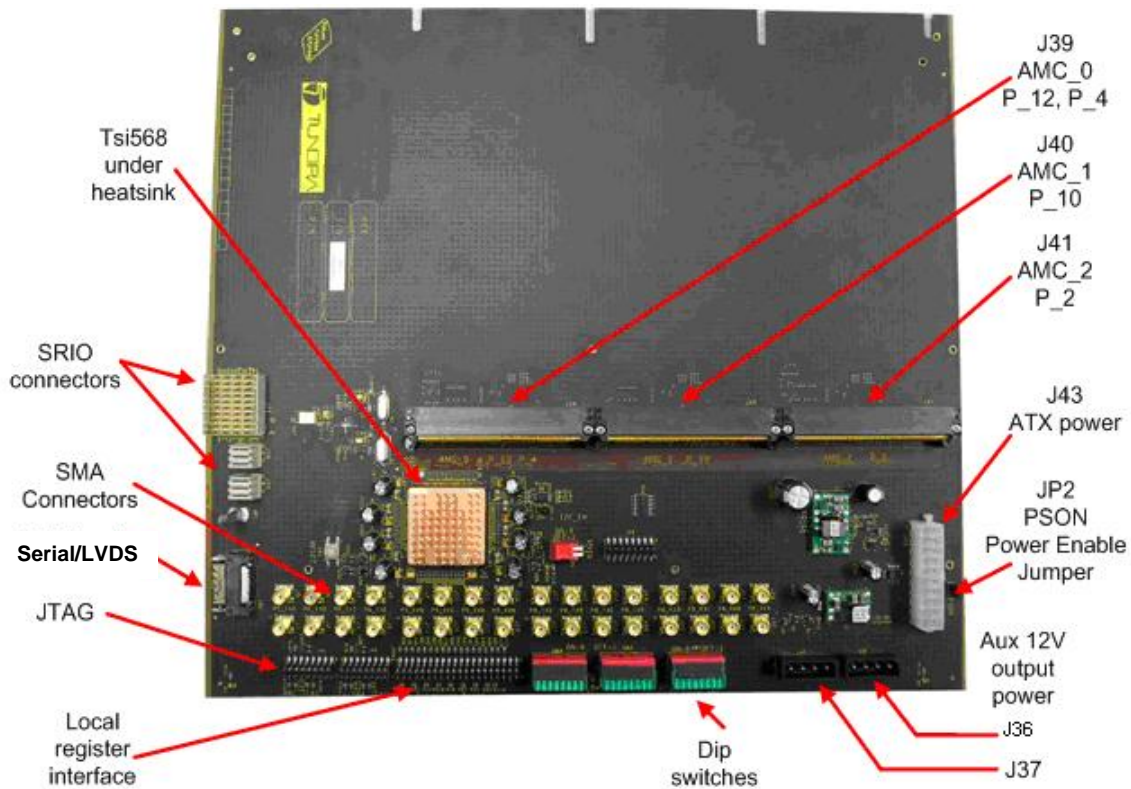


Figure 1 – SRDP Card Top View

Figure 2 shows the bottom side of the SRDP and identifies locations for the mounting hardware that is supplied with the board.

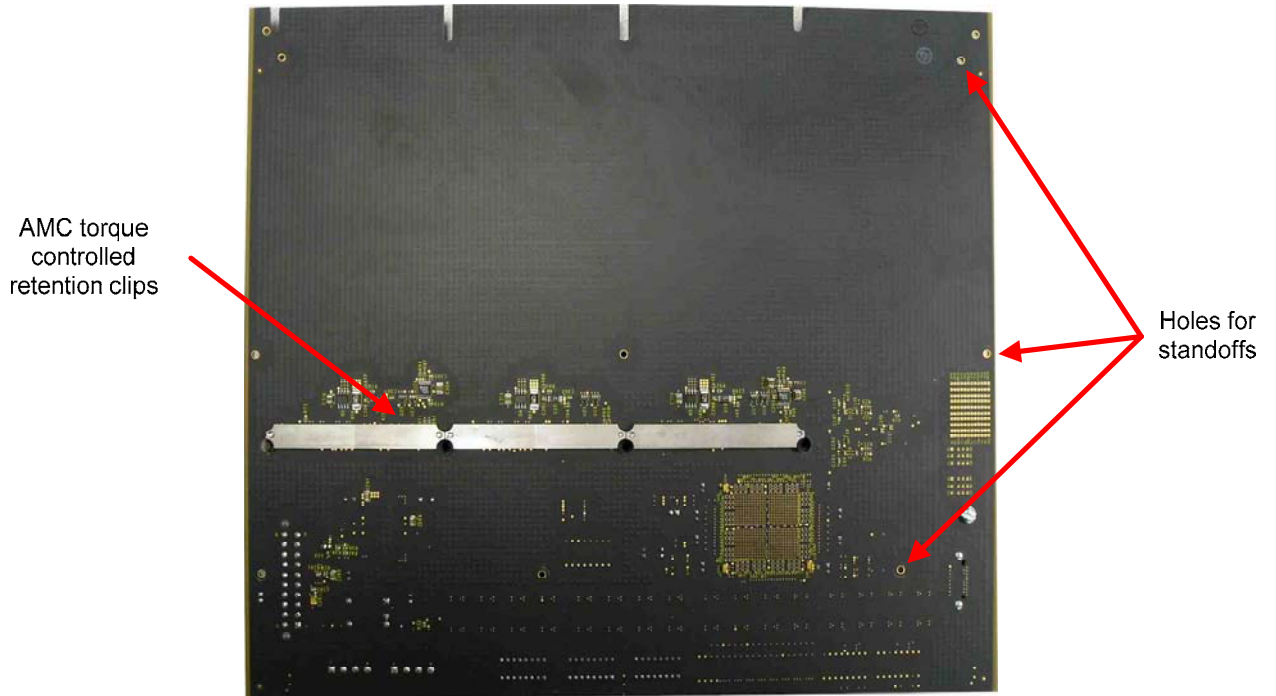


Figure 2 – SRDP Card Bottom View

1.2 Power Connectors

This section will provide a general description of the multiple power connectors, their function and associated pin numbers on the SRDP board. Refer to Figure 1 for connector locations.

1.2.1 J43 – ATX Input Power Connector

Pin Number	Description
1	3.3V
2	3.3V
3	GND
4	5.0V
5	GND
6	5.0V
7	GND
8	PWROK – (no connect)
9	No connect
10	12V
11	3.3V
12	-12V – (no connect)
13	GND

14	PSON – Power On – Connected to JP2
15	GND
16	GND
17	GND
18	-5.0V – (no connect)
19	5.0V
20	5.0V

1.2.2 J36 and J37 – Auxiliary Output Power Connectors

The Auxiliary Output Power Connector provides the power for any peripheral device.

Pin Number	J36	J37
1	+12V	+12V
2	GND	GND
3	GND	GND
4	No connect	No connect

1.2.3 JP2 – PSON/Power Enable Jumper (ATX Power Enable)

An external ATX power supply needs a feedback signal from the SRDP board before supplying power to the board. The purpose of the JP2 jumper is to provide an enable signal for the ATX power supply to power the board. If the JP2 jumper is not installed, the power supply will not provide power to the board.

1.2.4 System Reset Switch SW1

The reset switch SW1 applies a system reset to the following devices and interfaces:

- AMC Connector J39-B41
- AMC Connector J40-B41
- AMC Connector J41-B41
- Test Connector J38-16
- Tsi568A Hard Reset pin AF2 (U1)
- Tsi568A JTAG reset pin AE26 (U1)

1.2.5 SMA Connector Port Allocation

1.2.5.1 Serial Port 0

SMA Jack	Tsi568A pin name	Tsi568A Ball num	Differential Pair	Description
			TRANSMIT	
J1	SP0_TA_p	C2	P0_TXA	Port 0 Lane A non-inverting Transmit Data output.
J5	SP0_TA_n	C1	P0_TXA	Port 0 Lane A inverting Transmit Data output.
J2	SP0_TB_p	E1	P0_TXB	Port 0 Lane B non-inverting Transmit Data output.

J6	SP0_TB_n	E2	P0_TXB	Port 0 Lane B inverting Transmit Data output.
J3	SP0_TC_p	G2	P0_TXC	Port 0 Lane C non-inverting Transmit Data output.
J7	SP0_TC_n	G1	P0_TXC	Port 0 Lane C inverting Transmit Data output.
J4	SP0_TD_p	J1	P0_TXD	Port 0 Lane D non-inverting Transmit Data output.
J8	SP0_TD_n	J2	P0_TXD	Port 0 Lane D inverting Transmit Data output.
			RECEIVE	
J16	SP0_RA_p	C4	P0_RXA	Port 0 Lane A non-inverting Receive Data input.
J12	SP0_RA_n	C5	P0_RXA	Port 0 Lane A inverting Receive Data input.
J15	SP0_RB_p	E5	P0_RXB	Port 0 Lane B non-inverting Receive Data input.
J11	SP0_RB_n	E4	P0_RXB	Port 0 Lane B inverting Receive Data input.
J14	SP0_RC_p	G4	P0_RXC	Port 0 Lane C non-inverting Receive Data input.
J10	SP0_RC_n	G5	P0_RXC	Port 0 Lane C inverting Receive Data input.
J13	SP0_RD_p	J5	P0_RXD	Port 0 Lane D non-inverting Receive Data input.
J9	SP0_RD_n	J4	P0_RXD	Port 0 Lane D inverting Receive Data input.

1.2.5.2 Serial Port 8

SMA Jack	Tsi568A pin name	Tsi568A ball num	Differential Pair	Description
			TRANSMIT	
J17	SP8_TA_p	L2	P8_TXA	Port 8 Lane A non-inverting Transmit Data output.
J21	SP8_TA_n	L1	P8_TXA	Port 8 Lane A inverting Transmit Data output.
J18	SP8_TB_p	N1	P8_TXB	Port 8 Lane B non-inverting Transmit Data output.
J22	SP8_TB_n	N2	P8_TXB	Port 8 Lane B inverting Transmit Data output.
J19	SP8_TC_p	R2	P8_TXC	Port 8 Lane C non-inverting Transmit Data output.
J23	SP8_TC_n	R1	P8_TXC	Port 8 Lane C inverting Transmit Data output.
J20	SP8_TD_p	U1	P8_TXD	Port 8 Lane D non-inverting Transmit Data output.
J24	SP8_TD_n	U2	P8_TXD	Port 8 Lane D inverting Transmit Data output.
			RECEIVE	
J32	SP8_RA_p	L4	P8_RXA	Port 8 Lane A non-inverting Receive Data input.
J28	SP8_RA_n	L5	P8_RXA	Port 8 Lane A inverting Receive Data input.
J31	SP8_RB_p	N5	P8_RXB	Port 8 Lane B non-inverting Receive Data input.
J27	SP8_RB_n	N4	P8_RXB	Port 8 Lane B inverting Receive Data input.
J30	SP8_RC_p	R4	P8_RXC	Port 8 Lane C non-inverting Receive Data input.
J26	SP8_RC_n	R5	P8_RXC	Port 8 Lane C inverting Receive Data input.
J29	SP8_RD_p	U5	P8_RXD	Port 8 Lane D non-inverting Receive Data input.
J25	SP8_RD_n	U4	P8_RXD	Port 8 Lane D inverting Receive Data input.

1.2.6 J42 - Serial/LVDS Port Allocation

J42 - Serial Port 14

Tsi568A pin name	Tsi568A ball num	J42 pin name	J42 Pin num	Description
		TRANSMIT		
SP14_TA_p	B13	IB0_TA_P	S16	Port 14 Lane A non-inverting Transmit Data output.
SP14_TA_n	A13	IB0_TA_N	S15	Port 14 Lane A inverting Transmit Data output.
SP14_TB_p	A11	IB0_TB_P	S14	Port 14 Lane B non-inverting Transmit Data output.
SP14_TB_n	B11	IB0_TB_N	S13	Port 14 Lane B inverting Transmit Data output.
SP14_TC_p	B9	IB0_TC_P	S12	Port 14 Lane C non-inverting Transmit Data output.
SP14_TC_n	A9	IB0_TC_N	S11	Port 14 Lane C inverting Transmit Data output.
SP14_TD_p	A7	IB0_TD_P	S10	Port 14 Lane D non-inverting Transmit Data output.
SP14_TD_n	B7	IB0_TD_N	S9	Port 14 Lane D inverting Transmit Data output.
		RECEIVE		
SP14_RA_p	D13	IB0_RA_P	S1	Port 14 Lane A non-inverting Receive Data input.
SP14_RA_n	E13	IB0_RA_N	S2	Port 14 Lane A inverting Receive Data input.
SP14_RB_p	E11	IB0_RB_P	S3	Port 14 Lane B non-inverting Receive Data input.
SP14_RB_n	D11	IB0_RB_N	S4	Port 14 Lane B inverting Receive Data input.
SP14_RC_p	D9	IB0_RC_P	S5	Port 14 Lane C non-inverting Receive Data input.
SP14_RC_n	E9	IB0_RC_N	S6	Port 14 Lane C inverting Receive Data input.
SP14_RD_p	E7	IB0_RD_P	S7	Port 14 Lane D non-inverting Receive Data input.
SP14_RD_n	D7	IB0_RD_N	S8	Port 14 Lane D inverting Receive Data input.

1.2.7 J33 - Serial RIO Interface Port Allocation

J33 - Serial Port 6

Tsi568A pin name	Tsi568A ball num	J33 pin name	J33 Pin num	Description
		TRANSMIT		
SP6_TA_p	B21	P_TD0	A1	Port 6 Lane A non-inverting Transmit Data output.
SP6_TA_n	A21	N_TD0	B1	Port 6 Lane A inverting Transmit Data output.
SP6_TB_p	A19	P_TD1	A2	Port 6 Lane B non-inverting Transmit Data output.
SP6_TB_n	B19	N_TD1	B2	Port 6 Lane B inverting Transmit Data output.
SP6_TC_p	B17	P_TD2	A3	Port 6 Lane C non-inverting Transmit Data output.
SP6_TC_n	A17	N_TD2	B3	Port 6 Lane C inverting Transmit Data output.
SP6_TD_p	A15	P_TD3	A4	Port 6 Lane D non-inverting Transmit Data output.
SP6_TD_n	B15	N_TD4	B4	Port 6 Lane D inverting Transmit Data output.
		RECEIVE		
SP6_RA_p	D21	P_RD0	H10	Port 6 Lane A non-inverting Receive Data input.
SP6_RA_n	E21	N_RD0	G10	Port 6 Lane A inverting Receive Data input.

SP6_RB_p	E19	P_RD1	H9	Port 6 Lane B non-inverting Receive Data input.
SP6_RB_n	D19	N_RD1	G9	Port 6 Lane B inverting Receive Data input.
SP6_RC_p	D17	P_RD2	H8	Port 6 Lane C non-inverting Receive Data input.
SP6_RC_n	E17	N_RD2	G8	Port 6 Lane C inverting Receive Data input.
SP6_RD_p	E15	P_RD3	H7	Port 6 Lane D non-inverting Receive Data input.
SP6_RD_n	D15	N_RD4	G7	Port 6 Lane D inverting Receive Data input.

1.2.8 J34 – Power

Voltage Level	Pin Numbers
3.3V	A1 to A4, B1 to B4
ground	C1 to C4

1.2.9 J35 - Power

Voltage Level	Pin Numbers
5V	B1 to B4, C1 to C4
ground	A1 to A4

1.2.10 Configuration/Programming

Switches SW2 & SW4 control the Power-Down State of each Transmit and Receive Port. Changes are effected only following a reset of the Tsi568A device. Individual Serial RapidIO ports may be powered down to reduce the overall power consumption of the SRDP.

It should be noted that the Power-Down State may also be set externally via the J44 connector; however these switches must be set in the OFF position for J44 operation. The function of each switch is described below.

NOTE: Failure to follow this note may result in improper results from the board.

All configuration switch changes do not take effect until a HW_RST is applied to the Tsi568A.

1.2.10.1 SW2 – Power Down Configuration Dipswitch

ON = closed = switch down = 0 = GND

OFF = open = switch up = 1 = 10k pull-up to 3.3V

Tsi568A pin name	Tsi568 A ball num	SW2 switch num	J44 Pin num	Description
SP8_PWRDWN	Y1	1	18	Port 8 Tx and Rx power down control Controls the state all four lanes of Port 8 and Port 9. ON: Port 8 Powered Up, Port 9 controlled by SP9_PWRDWN OFF: Port 8 Powered Down, Port 9 Powered Down
SP9_PWRDWN	Y3	2	20	Port 9 Tx and Rx power down control Controls the state of Port 9. Note: Port 9 is never used when 4X mode is selected for Port 8 Serial Rapid IO MAC and it must be powered down. ON: Port 9 Powered Up OFF: Port 9 Powered Down
SP10_PWRDWN	Y4	3	22	Port 10 Tx and Rx power down control Controls the state all four lanes of Port 10 and Port 11. ON: Port 10 Powered Up, Port 11 controlled by SP11_PWRDWN OFF: Port 10 Powered Down, Port 11 Powered Down
SP11_PWRDWN	Y6	4	24	Port 11 Tx and Rx power down control Controls the state of Port 11. Note: Port 11 is never used when 4X mode is selected for Port 10 Serial Rapid IO MAC and it must be powered down. ON: Port 11 Powered Up OFF: Port 11 Powered Down
SP12_PWRDWN	AA2	5	26	Port 12 Tx and Rx power down control Controls the state all four lanes of Port 12 and Port 13. ON: Port 12 Powered Up, Port 13 controlled by SP13_PWRDWN OFF: Port 12 Powered Down, Port 13 Powered Down
SP13_PWRDWN	AA3	6	28	Port 13 Tx and Rx power down control Controls the state of Port 13. Note: Port 13 is never used when 4X mode is selected for Port 12 Serial Rapid IO MAC and it must be powered down. ON: Port 13 Powered Up OFF: Port 13 Powered Down
SP14_PWRDWN	W7	7	30	Port 14 Tx and Rx power down control Controls the state all four lanes of Port 14 and Port 15. ON: Port 14 Powered Up, Port 15 controlled by SP15_PWRDWN OFF: Port 14 Powered Down, Port 15 Powered Down

SP15_PWRDWN	Y8	8	32	Port 15 Tx and Rx power down control Controls the state of Port 15. Note: Port 15 is never used when 4X mode is selected for Port 14 Serial Rapid IO MAC and it must be powered down. ON: Port 15 Powered Up OFF: Port 15 Powered Down
-------------	----	---	----	---

1.2.10.2 SW4 – Power Down Configuration Dipswitch

ON = closed = switch down = 0 = GND

OFF = open = switch up = 1 = 10k pull-up to 3.3V

Tsi568A pin name	Tsi568A ball num	SW4 switch num	J44 Pin num	Description
SP0_PWRDWN	AE22	1	2	Port 0 Tx and Rx power down control Controls the state all four lanes of Port 0 and Port 1. ON: Port 0 Powered Up, Port 1 controlled by SP1_PWRDWN OFF: Port 0 Powered Down, Port 1 Powered Down
SP1_PWRDWN	AF22	2	4	Port 1 Tx and Rx power down control Controls the state of Port 1. Note: Port 1 is never used when 4X mode is selected for Port 0 Serial Rapid IO MAC and it must be powered down. ON: Port 1 Powered Up OFF: Port 1 Powered Down
SP2_PWRDWN	AE23	3	6	Port 2 Tx and Rx power down control Controls the state all four lanes of Port 2 and Port 3. ON: Port 2 Powered Up, Port 3 controlled by SP3_PWRDWN OFF: Port 2 Powered Down, Port 3 Powered Down
SP3_PWRDWN	AF23	4	8	Port 3 Tx and Rx power down control Controls the state of Port 3. Note: Port 3 is never used when 4X mode is selected for Port 2 Serial Rapid IO MAC and it must be powered down. ON: Port 3 Powered Up OFF: Port 3 Powered Down
SP4_PWRDWN	W2	5	10	Port 4 Tx and Rx power down control Controls the state all four lanes of Port 4 and Port 5. ON: Port 4 Powered Up, Port 5 controlled by SP5_PWRDWN OFF: Port 4 Powered Down, Port 5 Powered Down

SP5_PWRDWN	W3	6	12	Port 5 Tx and Rx power down control Controls the state of Port 5. Note: Port 5 is never used when 4X mode is selected for Port 4 Serial Rapid IO MAC and it must be powered down. ON: Port 5 Powered Up OFF: Port 5 Powered Down
SP6_PWRDWN	W5	7	14	Port 6 Tx and Rx power down control Controls the state all four lanes of Port 6 and Port 7. ON: Port 6 Powered Up, Port 7 controlled by SP7_PWRDWN OFF: Port 6 Powered Down, Port 7 Powered Down
SP7_PWRDWN	W6	8	16	Port 7 Tx and Rx power down control Controls the state of Port 7. Note: Port 7 is never used when 4X mode is selected for Port 6 Serial Rapid IO MAC and it must be powered down. ON: Port 7 Powered Up OFF: Port 7 Powered Down

1.2.11 SW3 – Mode Select Programming Dipswitch

SW3 controls the operating Mode of each of the Ports. Changes are effected only following a reset of the Tsi568A device. It should be noted that the Mode may also be set externally via the J44 connector; however these switches must be set in the OFF position for J44 operation. The function of each switch is enumerated below.

ON = closed = switch down = 0 = GND

OFF = open = switch up = 1 = 10k pull-up to 3.3V

Tsi568A pin name	Tsi568 A ball num	SW3 switch num	J44 Pin num	Description
SP0_MODESEL	AD22	1	1	PORT 0/1 Operating Mode This switch controls the Mode for Ports 0 and Port 1. ON: Port 0 operating in 4X mode (Port 1 not available) OFF: Ports 0 and 1 operating in 1X mode
SP2_MODESEL	AD23	2	5	PORT 2/3 Operating Mode This switch controls the Mode for Ports 2 and Port 3. ON: Port 2 operating in 4X mode (Port 3 not available) OFF: Ports 2 and 3 operating in 1X mode

SP4_MODESEL	AB1	3	9	<p>PORT 4/5 Operating Mode This switch controls the Mode for Ports 4 and Port 5.</p> <p>ON: Port 4 operating in 4X mode (Port 5 not available) OFF: Ports 4 and 5 operating in 1X mode</p>
SP6_MODESEL	AB3	4	13	<p>PORT 6/7 Operating Mode This switch controls the Mode for Ports 6 and Port 7.</p> <p>ON: Port 6 operating in 4X mode (Port 7 not available) OFF: Ports 6 and 7 operating in 1X mode</p>
SP8_MODESEL	AB4	5	17	<p>PORT 8/9 Operating Mode This switch controls the Mode for Ports 8 and Port 9.</p> <p>ON: Port 8 operating in 4X mode (Port 9 not available) OFF: Ports 8 and 9 operating in 1X mode</p>
SP10_MODESEL	AC3	6	21	<p>PORT 10/11 Operating Mode This switch controls the Mode for Ports 10 and Port 11.</p> <p>ON: Port 10 operating in 4X mode (Port 11 not available) OFF: Ports 10 and 11 operating in 1X mode</p>
SP12_MODESEL	AF3	7	25	<p>PORT 12/13 Operating Mode This switch controls the Mode for Ports 12 and Port 13.</p> <p>ON: Port 12 operating in 4X mode (Port 13 not available) OFF: Ports 12 and 13 operating in 1X mode</p>
SP14_MODESEL	AF4	8	29	<p>PORT 14/15 Operating Mode This switch controls the Mode for Ports 14 and Port 15.</p> <p>ON: Port 14 operating in 4X mode (Port 15 not available) OFF: Ports 14 and 15 operating in 1X mode</p>

1.2.12 SW5 – Speed Configuration Dipswitch

SW5 controls the Serial Port Transmit and Receive Operating Frequency, and selects the speed at which the port operates. The output data rate per lane is 10 times the selected input clock. Changes are effected only following a reset of the Tsi568A device. It should be noted that the Operating Frequency may also be set externally via the J44

connector; however these switches must be set in the OFF position for J44 operation. The function of each switch is enumerated below.

SW5-2	SW5-1	Description
Speed 1	Speed 0	
OFF	OFF	Reserved
OFF	ON	3.125 Gbaud
ON	OFF	2.50 Gbaud
ON	ON	1.25 Gbaud

ON = closed = switch down = 0 = GND

OFF = open = switch up = 1 = 10k pull-up to 3.3V

Tsi568A pin name	Tsi568A ball num	SW5 switch num	J44 Pin num	Description
Tsi568A_SPEED0	AC22	1	34	Serial port Tx and Rx operating frequency select bit 0
Tsi568A_SPEED1	AC23	2	36	Serial port Tx and Rx operating frequency select bit 1

1.2.13 J44 – External Control Port

J44 provides a means to externally control and configure the Serial Rapid IO Evaluation Card. This interfaces provides control of the Tsi568A Power Down, Mode Select, Operating Frequency and Reset. This interface also provides an interface the 2-wire serial bus for each AMC card. A description of each signal is described in the table below.

NOTE: Failure to follow this note may result in improper results from the board.

All configuration signal changes do not take effect until a HW_RST is applied to the Tsi568A.

Tsi568A pin name	Tsi568A ball num	switch num	J44 Pin num	Description
SP0_MODESEL	AD22	SW3-1	1	<p>SP0_MODESEL - PORT 0/1 Operating Mode This signal controls the Mode for Ports 0 and Port 1.</p> <p>0: Port 0 operating in 4X mode (Port 1 not available) 1: Ports 0 and 1 operating in 1X mode</p> <p>Note: SW3-1 must be in the OFF position to use this external control signal.</p>
SP0_PWRDWN	AE22	SW4-1	2	<p>SP0_PWRDN - PORT 0 Transmit & Receive Power Down Control. This signal controls the state all four lanes of Port 0 and Port 1.</p> <p>0: Port 0 Powered Up, Port 1 controlled by SP1_PWRDN 1: Port 0 Powered Down, Port 1 Powered Down</p> <p>Note: SW4-1 must be in the OFF position to use this external control signal.</p>
			3	Signal Ground
SP1_PWRDWN	AF22	SW4-2	4	<p>SP1_PWRDN - PORT 1 Transmit & Receive Power Down Control. This signal controls the state of Port 1. Note: Port 1 is never used when 4X mode is selected for Port 0 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 1 Powered Up 1: Port 1 Powered Down.</p> <p>Note: SW4-2 must be in the OFF position to use this external control signal.</p>

Tsi568A pin name	Tsi568A ball num	switch num	J44 Pin num	Description
SP2_MODESEL	AD23	SW3-2	5	<p>SP2_MODESEL - PORT 2/3 Operating Mode This signal controls the Mode for Ports 2 and Port 3.</p> <p>0: Port 2 operating in 4X mode (Port 3 not available) 1: Ports 2 and 3 operating in 1X mode</p> <p>Note: SW3-2 must be in the OFF position to use this external control signal.</p>
SP2_PWRDWN	AE23	SW4-3	6	<p>SP2_PWRDN - PORT 2 Transmit & Receive Power Down Control. This signal controls the state all four lanes of Port 2 and Port 3.</p> <p>0: Port 2 Powered Up, Port 3 controlled by SP3_PWRDN 1: Port 2 Powered Down, Port 3 Powered Down</p> <p>Note: SW4-3 must be in the OFF position to use this external control signal.</p>
			7	Signal Ground
SP3_PWRDWN	AF23	SW4-4	8	<p>SP3_PWRDN - PORT 3 Transmit & Receive Power Down Control. This signal controls the state of Port 3. Note: Port 3 is never used when 4X mode is selected for Port 2 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 3 Powered Up 1: Port 3 Powered Down</p> <p>Note: SW4-4 must be in the OFF position to use this external control signal.</p>
SP4_MODESEL	AB1	SW3-3	9	<p>SP4_MODESEL - PORT 4/5 Operating Mode This signal controls the Mode for Ports 4 and Port 5.</p> <p>0: Port 4 operating in 4X mode (Port 5 not available) 1: Ports 4 and 5 operating in 1X mode</p> <p>Note: SW3-3 must be in the OFF position to use this external control signal.</p>

Tsi568A pin name	Tsi568A ball num	switch num	J44 Pin num	Description
SP4_PWRDWN	W2	SW4-5	10	<p>SP4_PWRDWN - PORT 4 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 4 and Port 5.</p> <p>0: Port 4 Powered Up, Port 5 controlled by SP5_PWRDWN 1: Port 4 Powered Down, Port 5 Powered Down</p> <p>Note: SW4-5 must be in the OFF position to use this external control signal.</p>
			11	Signal Ground
SP5_PWRDWN	W3	SW4-6	12	<p>SP5_PWRDWN - PORT 5 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 5. Note: Port 5 is never used when 4X mode is selected for Port 4 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 5 Powered Up 1: Port 5 Powered Down</p> <p>Note: SW4-6 must be in the OFF position to use this external control signal.</p>
SP6_MODESEL	AB3	SW3-4	13	<p>SP6_MODESEL - PORT 6/7 Operating Mode</p> <p>This signal controls the Mode for Ports 6 and Port 7.</p> <p>0: Port 6 operating in 4X mode (Port 7 not available) 1: Ports 6 and 7 operating in 1X mode</p> <p>Note: SW3-4 must be in the OFF position to use this external control signal.</p>
SP6_PWRDWN	W5	SW4-7	14	<p>SP6_PWRDWN - PORT 6 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 6 and Port 7.</p> <p>0: Port 6 Powered Up, Port 7 controlled by SP7_PWRDWN 1: Port 6 Powered Down, Port 7 Powered Down</p> <p>Note: SW4-7 must be in the OFF position to use this external control signal.</p>

Tsi568A pin name	Tsi568A ball num	switch num	J44 Pin num	Description
			15	Signal Ground
SP7_PWRDWN	W6	SW4-8	16	<p>SP7_PWRDN - PORT 7 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 7. Note: Port 7 is never used when 4X mode is selected for Port 6 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 7 Powered Up 1: Port 7 Powered Down</p> <p>Note: SW4-8 must be in the OFF position to use this external control signal.</p>
SP8_MODESEL	AB4	SW3-5	17	<p>SP8_MODESEL - PORT 8/9 Operating Mode</p> <p>This signal controls the Mode for Ports 8 and Port 9.</p> <p>0: Port 8 operating in 4X mode (Port 9 not available) 1: Ports 8 and 9 operating in 1X mode</p> <p>Note: SW3-5 must be in the OFF position to use this external control signal.</p>
SP8_PWRDWN	Y1	SW2-1	18	<p>SP8_PWRDN - PORT 8 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 8 and Port 9.</p> <p>0: Port 8 Powered Up, Port 9 controlled by SP9_PWRDN 1: Port 8 Powered Down, Port 9 Powered Down</p> <p>Note: SW2-1 must be in the OFF position to use this external control signal.</p>
			19	Signal Ground

Tsi568A pin name	Tsi568A ball num	switch num	J44 Pin num	Description
SP9_PWRDWN	Y3	SW2-2	20	<p>SP9_PWRDN - PORT 9 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 9. Note: Port 9 is never used when 4X mode is selected for Port 8 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 9 Powered Up 1: Port 9 Powered Down</p> <p>Note: SW2-2 must be in the OFF position to use this external control signal.</p>
SP10_MODESEL	AC3	SW3-6	21	<p>SP10_MODESEL - PORT 10/11 Operating Mode</p> <p>This signal controls the Mode for Ports 10 and Port 11.</p> <p>0: Port 10 operating in 4X mode (Port 11 not available) 1: Ports 10 and 11 operating in 1X mode</p> <p>Note: SW3-6 must be in the OFF position to use this external control signal.</p>
SP10_PWRDWN	Y4	SW2-3	22	<p>SP10_PWRDN - PORT 10 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 10 and Port 11.</p> <p>0: Port 10 Powered Up, Port 11 controlled by SP11_PWRDN 1: Port 10 Powered Down, Port 11 Powered Down</p> <p>Note: SW2-3 must be in the OFF position to use this external control signal.</p>
			23	Signal Ground

Tsi568A pin name	Tsi568A ball num	switch num	J44 Pin num	Description
SP11_PWRDWN	Y6	SW2-4	24	<p>SP11_PWRDWN - PORT 11 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 11. Note: Port 11 is never used when 4X mode is selected for Port 10 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 11 Powered Up 1: Port 11 Powered Down</p> <p>Note: SW2-4 must be in the OFF position to use this external control signal.</p>
SP12_MODESEL	AF3	SW3-7	25	<p>SP12_MODESEL - PORT 12/13 Operating Mode</p> <p>This signal controls the Mode for Ports 12 and Port 13.</p> <p>0: Port 12 operating in 4X mode (Port 13 not available) 1: Ports 12 and 13 operating in 1X mode</p> <p>Note: SW3-7 must be in the OFF position to use this external control signal.</p>
SP12_PWRDWN	AA2	SW2-5	26	<p>SP12_PWRDWN - PORT 12 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 12 and Port 13.</p> <p>0: Port 12 Powered Up, Port 13 controlled by SP13_PWRDWN 1: Port 12 Powered Down, Port 13 Powered Down</p> <p>Note: SW2-5 must be in the OFF position to use this external control signal.</p>
			27	Signal Ground

Tsi568A pin name	Tsi568A ball num	switch num	J44 Pin num	Description
SP13_PWRDWN	AA3	SW2-6	28	<p>SP13_PWRDWN - PORT 13 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 13. Note: Port 13 is never used when 4X mode is selected for Port 12 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 13 Powered Up 1: Port 13 Powered Down</p> <p>Note: SW2-6 must be in the OFF position to use this external control signal.</p>
SP14_MODESEL	AF4	SW3-8	29	<p>SP14_MODESEL - PORT 14/15 Operating Mode</p> <p>This signal controls the Mode for Ports 14 and Port 15.</p> <p>0: Port 14 operating in 4X mode (Port 15 not available) 1: Ports 14 and 15 operating in 1X mode</p> <p>Note: SW3-8 must be in the OFF position to use this external control signal.</p>
SP14_PWRDWN	W7	SW2-7	30	<p>SP14_PWRDWN - PORT 14 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 14 and Port 15.</p> <p>0: Port 14 Powered Up, Port 15 controlled by SP15_PWRDWN 1: Port 14 Powered Down, Port 15 Powered Down</p> <p>Note: SW2-7 must be in the OFF position to use this external control signal.</p>
HARD_RST_B	AF2		31	<p>Active low Tsi568A Hardware Reset. Must be held low for a minimum of 1 ms.</p>

Tsi568A pin name	Tsi568A ball num	switch num	J44 Pin num	Description
SP15_PWRDWN	Y8	SW2-8	32	<p>SP15_PWRDWN - PORT 15 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 15. Note: Port 15 is never used when 4X mode is selected for Port 14 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 15 Powered Up 1: Port 15 Powered Down</p> <p>Note: SW2-8 must be in the OFF position to use this external control signal.</p>
n/a	n/a	n/a	33	AMC 0, IPMB-L Clock. This signal is the IPMB-L I ² C Clock for AMC Port 0.
Tsi568A_SPEED 0	AC22	SW5-1	34	<p>See Tsi568A_SPEED0 (pin 36)</p> <p>Note: SW5-1 must be in the OFF position to use this external control signal.</p>
n/a	n/a	n/a	35	AMC 0, IPMB-L Data. This signal is the IPMB-L I ² C Data for AMC Port 0.
Tsi568A_SPEED 1	AC23	SW5-2	36	<p>Serial Port Transmit and Receive Operating Frequency. In conjunction with Tsi568A_SPEED0 selects the speed at which the ports operate. The output data rate per lane is 10 times the selected input clock. Changes are effected only following a reset of the Tsi568A device. The function of each signal is enumerated below.</p> <p>See SW5 Table for setting data rate.</p> <p>Note: SW5-2 must be in the OFF position to use this external control signal.</p>
n/a	n/a	n/a	37	AMC 1, IPMB-L Clock. This signal is the IPMB-L I ² C Clock for AMC Port 1.
n/a	n/a	n/a	38	AMC 2, IPMB-L Clock. This signal is the IPMB-L I ² C Clock for AMC Port 2.
n/a	n/a	n/a	39	AMC 1, IPMB-L Data. This signal is the IPMB-L I ² C Data for AMC Port 1.
n/a	n/a	n/a	40	AMC 2, IPMB-L Data. This signal is the IPMB-L I ² C Data for AMC Port 2.

1.2.14 JTAG Headers

The SRDP supports JTAG programming of the Tsi568A through the JTAG connector J45 as well as through peripheral devices on AMC cards through the AMC TJAG connector J46.

1.2.14.1 J45 - Tsi568A JTAG Header

Tsi568A pin name	Tsi568A ball num	J45 Pin num	Description
TDO	AD25	1	Tsi568A TDO
		2	No connect
TDI	AD26	3	Tsi568A TDI
TRST_B	AE26	4	Tsi568A TRST
		5	No connect
		6	3.3V
TCK	AF26	7	Tsi568A TCK
		8	No connect
TMS	AC26	9	Tsi568A TMS
		10	No connect
		11	No connect
		12	GND
		13	No connect
		14	No connect
		15	No connect
		16	GND

1.2.14.2 J46 - AMC JTAG Header

AMC Header pin name	AMC Pin num	J46 Pin num	Description
AMC_CHN1	J39-B169	1	AMC Interface 0 pin B169
		2	No connect
AMC_CHN4	J41-B169	3	AMC Interface 2 pin B169
AMC_TRST	B167	4	TRST for AMC interface 0 to 2
		5	No connect
		6	3.3V
AMC_TCK	B165	7	TCK for AMC interface 0 to 2
		8	No connect
AMC_TMS	B166	9	TMS for AMC interface 0 to 2
		10	No connect
		11	No connect
		12	GND
		13	No connect
		14	No connect
		15	No connect
		16	GND

1.2.15 J38 - External Status Port

J38 provides a means for external access to the system status signals. The table below describes the function of each pin.

J38 PIN	SIGNAL	DESCRIPTION
1	Not used	
2	Tsi568A_INT	Tsi568A Interrupt signal.
3	Not used	
4	Tsi568A_SW_RST	Tsi568A Software reset. This signal is asserted when a Rapid IO port valid reset request on a Rapid IO link. If self reset is not selected, this signal remains asserted until the reset request is cleared from the status registers. If self reset is selected, this pin remains asserted until the self reset is complete. If the Tsi568A is reset from the HARD_RESET_b pin, this pin is de-asserted and remains de-asserted after HARD_RESET_b is released.
5	Not used	
6	EN_1V2_N	Active low signal indicating that both the 12V and 3.3V power rails are active and within specified limits. Note: this signal is at 5V CMOS levels.
7	Not used	
8	1V2_GOOD	Active high signal indicating that the 1.2V power is active and within specified limits. Note: this signal is at 5V CMOS levels.
9	Not used	
10	1V5_GOOD	Active high signal indicating that the 1.5V power is active and within specified limits. Note: this signal is at 5V CMOS levels.
11	Not used	
12	Not used	
13	Not used	
14	Not used	
15	Signal Ground	
16	SYS_RESET_N	Active low System Reset. This signal is active for a minimum of 1 ms. Note: this signal is at 3.3V CMOS levels.

2.0 SRDP HARDWARE DESIGN & ARCHITECTURE

2.1 General Description

Some of the features and characteristics of the SRDP are:

- 80 Gbits/s aggregate bandwidth
- More processing power-per-watt via distributed CPUs
- Highly configurable
- Low power consumption
- Compliant to RapidIO Specification (Revision 1.2)

Typical Applications for Serial RIO

- System level solutions with Qos demands
- Mesh networking, wired or wireless
- Multiprocessor systems
- ASIC/SOC/IP development
- Deterministic board to board solutions
- Low overhead SMP implementations

2.2 Physical Specifications

Board Size.....	302 x 322mm
Power Requirements.....	Standard ATX Supply
Operating Temperature.....	0° to 70°C
Standards Compliance.....	RapidIO Specifications (Rev 1.2)
Weight.....	1.5Kg
RoHS.....	Compliant

Figure 3 below is a block diagram of the Tsi568A switch and how it interfaces to the associated connectors supported on the SRDP board.

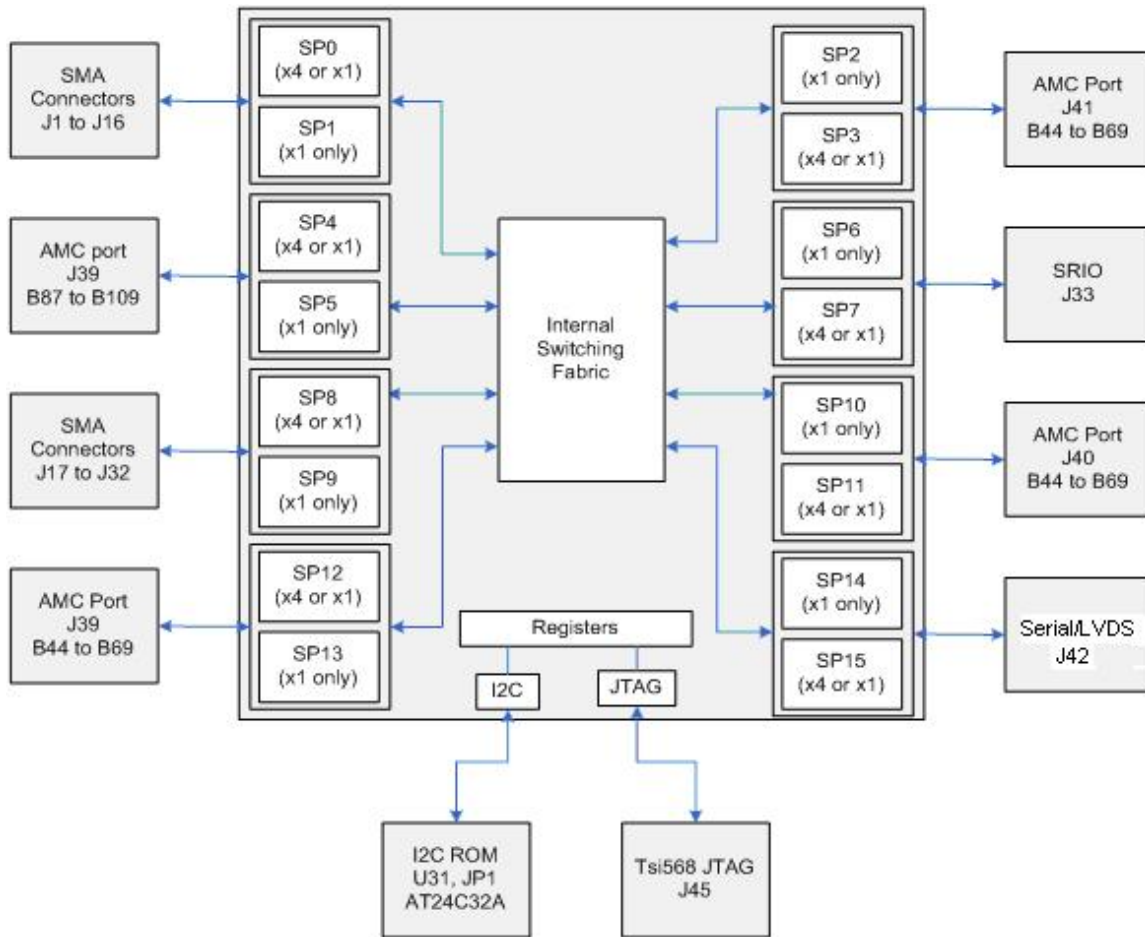


Figure 3 – Block Diagram

2.3 Hardware Configuration

The SRDP has user configurable options which include:

- Programmable Clocking
- Port Speed
- External EEPROM access
- Serial RapidIO port mode select
- Power Down options.

2.3.1 Clocking and Port Speed

The SRDP can support the multiple reference clocks that the Tsi568A chip is capable of using. These are Tsi568A S_CLK1 and Tsi568A S_CLK2.

2.3.1.1 S_CLK1

Selection jumper JP5 must be installed if an external clock generator is to be used. It is connected to SMA J55 and provides the input source for Tsi568A S_CLK1. If JP5 is not installed then the on-board clock circuitry provides the clocking signal.

NOTE: Failure to follow this note may result in improper results from the board.

The Tsi568A S_CLK1 operates at 312.5MHz. The signal source should be at LVCMOS/LVTTL levels.

Frequency Selection Jumper JP6 must be properly set for either internal or external clock use. Refer to the table below for the correct configuration.

JP6	JP7	Frequency
Not installed	Not installed	312.5MHz Factory Default
Installed	Not installed	(external)

JP6 Selection Jumper Table

Output Enable Jumper JP4 enables the Tsi568A S_CLK1 outputs from the on-board clock generator to the SMA connectors J53 and J54 as well as the test points on connector JP3. These signals can be monitored with an oscilloscope connected to SMA connectors J53 and J54 or from a logic analyzer connected to JP3. The signal levels are LVPECL. These signals are only viewable when Jumper JP4 is installed.

The table below identifies the Tsi568A S_CLK1 pin assignments on connector JP3.

Pin Name	Signal Name
1	Tsi568A S_CLK1_p
2	Signal Ground
3	Tsi568A S_CLK1_n

JP3 Test Connector Table

2.3.1.2 S_CLK2

Selection jumper JP8 must be installed if an external clock generator is to be used. If JP8 is not installed then the on-board clock circuitry provides the clocking signal. The external clock frequency is applied to SMA connectors J58 and J59. JP8 installed is the factory default.

NOTE: Failure to follow this note may result in improper results from the board.

The Tsi568A S_CLK2 typically operates at 250MHz. The signal source should be at LVCMOS/LVTTL levels.

The On-board Frequency Disable Jumper JP9 disables the on-board clock generator when installed. If not installed then the On-board clock generator provides the signal source to the Tsi568A. JP9 not installed is the factory default.

The table below identifies the Tsi568A S_CLK1 pin assignments on connector JP10.

Pin Name	Signal Name
1	Tsi568A S_CLK2_p
2	Signal Ground
3	Tsi568A S_CLK2_n

JP10 Test Connector Table

2.3.2 Port Speed Selection – SW5

Dipswitch SW5 determines the Port Speed selected. This switch controls the Serial RapidIO ports Transmit and Receive data rates.

The Serial RapidIO ports use source-clocked transmission which is embedded in the data stream using 8B/10B encoding. The Tsi568A decodes the embedded clock and generates a separate clock to transmit its own data.

The Tsi568A supports three difference signal rates that are generated from the two clock sources. The data rate is determined by the setting of the Serial RapidIO Port Speed Selection Dipswitch SW5. Refer to section 1.2.12 for details on the SW5 dipswitch settings.

NOTE: Failure to follow this note may result in improper results from the board.

The Serial RapidIO specification requires the transmit and receive signals to be at the same rate.

Additionally, the difference in speed between the transmit and receive clocks are +/- 200 parts per million maximum.

2.3.3 I²C External EEPROM Enable Jumper – JP1

With jumper JP1 installed, the Tsi568A can access the external EEPROM at boot-up after the chip receives a reset from the I²C interface. If the jumper is not installed, I²C register information must come from an external JTAG connection. JP1 not installed is the factory default.

2.3.3.1 I²C Interface

When the Tsi568A comes out of reset, the I²C Interface is responsible for performing automatic reads from an externally attached EEPROM device in order to load the initial configuration of the device. The Tsi568A I²C Interface issues an EEPROM reset immediately following the chip hardware reset (HARD_RST_b). The purpose of the EEPROM reset is to re-synchronize the serial EEPROM with the I²C Interface, after the interface has been reset.

The Tsi568A I²C Interface generates an EEPROM reset by pulling the SDA signal (I²C serial data line) high while putting out a sequence of nine pulses on SCLK signal (I²C serial clock). The nine SCLK pulses clear the I²C transaction that was in progress prior to the reset and provides one or more NACK signals. Following the ninth pulse, both the SDA signal and the SCLK signal are left high.

2.4 Logic Analyzer Test Connectors (J47 to J52)

These connectors provide a convenient logic analyzer interface to the following Serial RapidIO ports:

- Tsi568A Port 6: Serial/HIP Interface (J47)
- Tsi568A Port 12: AMC_0 (J48)
- Tsi568A Port 4: AMC_0 (J49)
- Tsi568A Port 10: AMC_1 (J50)
- Tsi568A Port 2: AMC_2 (J51)
- Tsi568A Port 14: Serial/LVDS (J52)

These industry standard interfaces provide the user a direct connection to standard logic analyzer compression-type probes. The table below shows the signal assignment on each interface.

The signals available are listed in the table below.

Pin Number	Signal	Pin Number	Signal
1	RA_p	2	GND
3	RA_n	4	TA_p
5	GND	6	TA_n
7	RB_p	8	GND
9	RB_n	10	TB_p
11	GND	12	TB_n
13	RC_p	14	GND
15	RC_n	16	TC_p
17	GND	18	TC_n
19	RD_p	20	GND
21	RD_n	22	TD_p
23	GND	24	TD_n

3.0 SRDP CONNECTIVITY & CONFIGURATION

This section contains general set-up information about the SRDP board. Refer to Figure 1 for jumper and switch locations.

3.1 Default Settings

Table 1 below defines the recommended default Jumper settings for the SRDP. Table 2 shows the recommended default Switch settings for the SRDP.

Settings of the jumpers and switches as shipped from STx may not reflect this set-up. Therefore it is recommended that you review these settings prior to powering the board up.

JUMPER	DESCRIPTION	DEFAULT SETTING
JP1	External EEPROM Access Jumper	Not installed
JP2	ATX Power Enable Jumper	Installed (enabled)
JP3	S_CLK1 Test Connector	N/A
JP4	S_CLK1 Test Clock Output Enable Jumper	Installed (enabled)
JP5	S_CLK1 Source Selection Jumper	Not installed
JP6	S_CLK1 On-board Source Frequency Selection Jumper 1	Not installed
JP7	S_CLK1 On-board Source Frequency Selection Jumper 2	Not Installed
JP8	S_CLK2 Source Selection Jumper	Not installed
JP9	S_CLK2 On-board Source Enable Jumper	Not installed
JP10	S_CLK2 Test Connector	N/A

Table 1 – Default Jumper Settings

DIP-SWITCH	DESCRIPTION	DEFAULT SETTING
SW1	Manual System Reset	Pushbutton (N/A)
SW2	Serial RapidIO Port Power Down Configurations	ON (Powered Up)
SW3	Serial RapidIO Port Mode Select	ON (All ports in 4x mode)
SW4	Serial RapidIO Port Power Down Configurations	ON (Powered Up)
SW5	Serial RapidIO Port Speed Selection	ON (1.25 Gbits/s bit rate)

Table 2 – Default Switch Settings

Appendix A – Schematics

See *file.pdf* for the complete schematics.