

Silicon Turnkey eXpress

Embedded Engineering Solutions

Serial RapidIO Development Platform for the Tundra Semiconductor Tsi578 Hardware Manual



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Revision History

Rev	Date	Comments
A	Nov. 1, 2006	Initial release of manual
B	Nov. 7, 2006	Change all Tsi578A to Tsi578, Sec 2.1 Compliant & Figure 3
C	Nov. 27, 2006	Revised SW4 and SW5 tables, Default Jumper table and JP6 jumper table renamed to JP7.
D	Dec. 4, 2006	Added notes to sections 1.2.10, 1.2.12, 1.2.13, 2.3.1.1, 2.3.3 and 3.1
E	Dec. 20, 2006	Replace Figure 1 and 2, update Figure 3. Change SW4 in Table 2 to OFF. Add NOTE to section 2.3.3.
F	Jan. 4, 2007	Add Appendix B

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The following information is intended to alert the user to possible dangers and important information contained within this guide. The **“WARNINGS”**, **“CAUTIONS”** and **“NOTES”** do not eliminate these dangers. Close attention to the information supplied along with “common sense” operation is the major accident prevention measure.

WARNING:	Failure to follow this warning may result in bodily injury.
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CAUTION:	Failure to follow this caution may result in possible damage to the board.
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NOTE:	Failure to follow this note may result in improper results from the board.
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1.0 GENERAL DESCRIPTION

The Serial RapidIO Development Platform (SRDP) is a standalone evaluation platform for Tundra Semiconductor's Tsi578 8-port Serial RapidIO Switch.

1.1 Device Placement

This section will provide a general description of the main components, connectors and switches associated with the Serial RapidIO Development Platform (SRDP).

Figure 1 below is an overall top view of the SRDP board and shows locations of the key components and connectors.

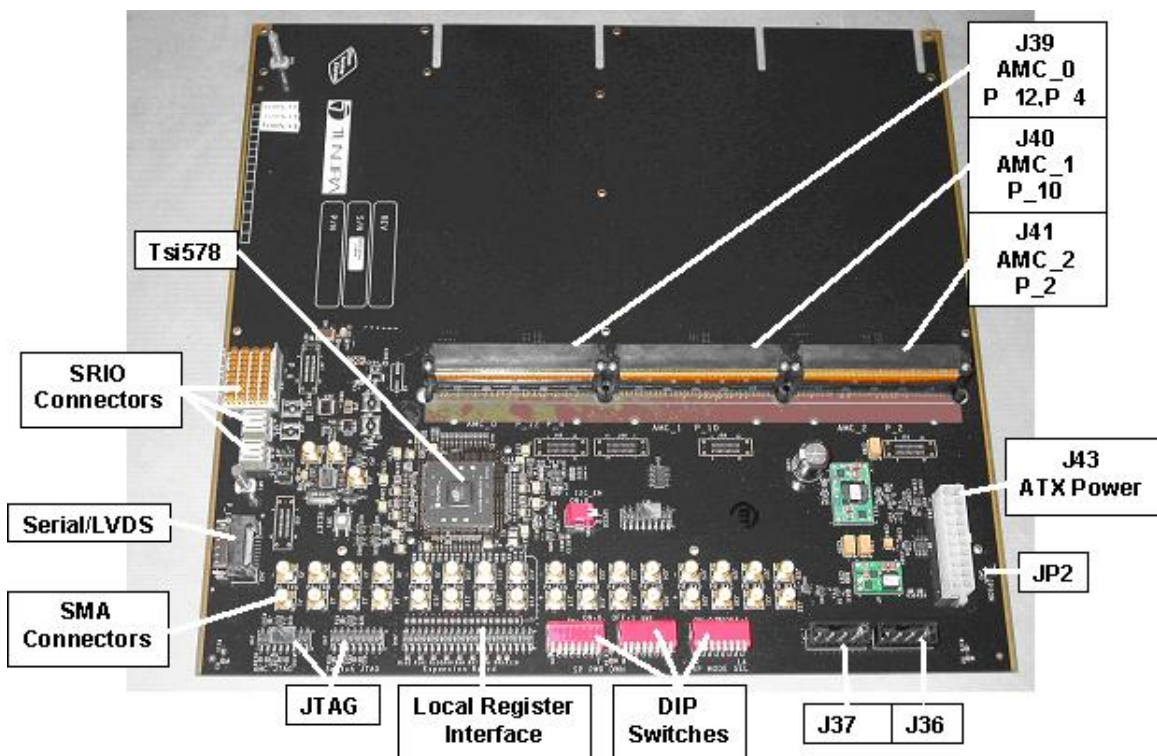


Figure 1 – SRDP Card Top View

8	PWROK – (no connect)
9	No connect
10	12V
11	3.3V
12	-12V – (no connect)
13	GND
14	PSON – Power On – Connected to JP2
15	GND
16	GND
17	GND
18	-5.0V – (no connect)
19	5.0V
20	5.0V

1.2.2 J36 and J37 – Auxiliary Output Power Connectors

The Auxiliary Output Power Connector provides the power for any peripheral device.

Pin Number	J36	J37
1	+12V	+12V
2	GND	GND
3	GND	GND
4	No connect	No connect

1.2.3 JP2 – PSON/Power Enable Jumper (ATX Power Enable)

An external ATX power supply needs a feedback signal from the SRDP board before supplying power to the board. The purpose of the JP2 jumper is to provide an enable signal for the ATX power supply to power the board. If the JP2 jumper is not installed, the power supply will not provide power to the board.

1.2.4 System Reset Switch SW1

The reset switch SW1 applies a system reset to the following devices and interfaces:

- AMC Connector J39-B41
- AMC Connector J40-B41
- AMC Connector J41-B41
- Test Connector J38-16
- Tsi578 Hard Reset pin AF2 (U1)
- Tsi578 JTAG reset pin AE26 (U1)

1.2.5 SMA Connector Port Allocation

1.2.5.1 Serial Port 0

SMA Jack	Tsi578 pin name	Tsi578 Ball num	Differential Pair	Description
			TRANSMIT	
J1	SP0_TA_p	C2	P0_TXA	Port 0 Lane A non-inverting Transmit Data output.
J5	SP0_TA_n	C1	P0_TXA	Port 0 Lane A inverting Transmit Data output.
J2	SP0_TB_p	E1	P0_TXB	Port 0 Lane B non-inverting Transmit Data output.
J6	SP0_TB_n	E2	P0_TXB	Port 0 Lane B inverting Transmit Data output.
J3	SP0_TC_p	G2	P0_TXC	Port 0 Lane C non-inverting Transmit Data output.
J7	SP0_TC_n	G1	P0_TXC	Port 0 Lane C inverting Transmit Data output.
J4	SP0_TD_p	J1	P0_TXD	Port 0 Lane D non-inverting Transmit Data output.
J8	SP0_TD_n	J2	P0_TXD	Port 0 Lane D inverting Transmit Data output.
			RECEIVE	
J16	SP0_RA_p	C4	P0_RXA	Port 0 Lane A non-inverting Receive Data input.
J12	SP0_RA_n	C5	P0_RXA	Port 0 Lane A inverting Receive Data input.
J15	SP0_RB_p	E5	P0_RXB	Port 0 Lane B non-inverting Receive Data input.
J11	SP0_RB_n	E4	P0_RXB	Port 0 Lane B inverting Receive Data input.
J14	SP0_RC_p	G4	P0_RXC	Port 0 Lane C non-inverting Receive Data input.
J10	SP0_RC_n	G5	P0_RXC	Port 0 Lane C inverting Receive Data input.
J13	SP0_RD_p	J5	P0_RXD	Port 0 Lane D non-inverting Receive Data input.
J9	SP0_RD_n	J4	P0_RXD	Port 0 Lane D inverting Receive Data input.

1.2.5.2 Serial Port 8

SMA Jack	Tsi578 pin name	Tsi578 ball num	Differential Pair	Description
			TRANSMIT	
J17	SP8_TA_p	L2	P8_TXA	Port 8 Lane A non-inverting Transmit Data output.
J21	SP8_TA_n	L1	P8_TXA	Port 8 Lane A inverting Transmit Data output.
J18	SP8_TB_p	N1	P8_TXB	Port 8 Lane B non-inverting Transmit Data output.
J22	SP8_TB_n	N2	P8_TXB	Port 8 Lane B inverting Transmit Data output.
J19	SP8_TC_p	R2	P8_TXC	Port 8 Lane C non-inverting Transmit Data output.
J23	SP8_TC_n	R1	P8_TXC	Port 8 Lane C inverting Transmit Data output.
J20	SP8_TD_p	U1	P8_TXD	Port 8 Lane D non-inverting Transmit Data output.
J24	SP8_TD_n	U2	P8_TXD	Port 8 Lane D inverting Transmit Data output.
			RECEIVE	
J32	SP8_RA_p	L4	P8_RXA	Port 8 Lane A non-inverting Receive Data input.
J28	SP8_RA_n	L5	P8_RXA	Port 8 Lane A inverting Receive Data input.
J31	SP8_RB_p	N5	P8_RXB	Port 8 Lane B non-inverting Receive Data input.
J27	SP8_RB_n	N4	P8_RXB	Port 8 Lane B inverting Receive Data input.
J30	SP8_RC_p	R4	P8_RXC	Port 8 Lane C non-inverting Receive Data input.
J26	SP8_RC_n	R5	P8_RXC	Port 8 Lane C inverting Receive Data input.
J29	SP8_RD_p	U5	P8_RXD	Port 8 Lane D non-inverting Receive Data input.
J25	SP8_RD_n	U4	P8_RXD	Port 8 Lane D inverting Receive Data input.

1.2.6 J42 - Serial/LVDS Port Allocation

J42 - Serial Port 14

Tsi578 pin name	Tsi578 ball num	J42 pin name	J42 Pin num	Description
		TRANSMIT		
SP14_TA_p	B13	IB0_TA_P	S16	Port 14 Lane A non-inverting Transmit Data output.
SP14_TA_n	A13	IB0_TA_N	S15	Port 14 Lane A inverting Transmit Data output.
SP14_TB_p	A11	IB0_TB_P	S14	Port 14 Lane B non-inverting Transmit Data output.
SP14_TB_n	B11	IB0_TB_N	S13	Port 14 Lane B inverting Transmit Data output.
SP14_TC_p	B9	IB0_TC_P	S12	Port 14 Lane C non-inverting Transmit Data output.
SP14_TC_n	A9	IB0_TC_N	S11	Port 14 Lane C inverting Transmit Data output.
SP14_TD_p	A7	IB0_TD_P	S10	Port 14 Lane D non-inverting Transmit Data output.
SP14_TD_n	B7	IB0_TD_N	S9	Port 14 Lane D inverting Transmit Data output.
		RECEIVE		
SP14_RA_p	D13	IB0_RA_P	S1	Port 14 Lane A non-inverting Receive Data input.
SP14_RA_n	E13	IB0_RA_N	S2	Port 14 Lane A inverting Receive Data input.
SP14_RB_p	E11	IB0_RB_P	S3	Port 14 Lane B non-inverting Receive Data input.
SP14_RB_n	D11	IB0_RB_N	S4	Port 14 Lane B inverting Receive Data input.
SP14_RC_p	D9	IB0_RC_P	S5	Port 14 Lane C non-inverting Receive Data input.
SP14_RC_n	E9	IB0_RC_N	S6	Port 14 Lane C inverting Receive Data input.
SP14_RD_p	E7	IB0_RD_P	S7	Port 14 Lane D non-inverting Receive Data input.
SP14_RD_n	D7	IB0_RD_N	S8	Port 14 Lane D inverting Receive Data input.

1.2.7 J33 - Serial RIO Interface Port Allocation

J33 - Serial Port 6

Tsi578 pin name	Tsi578 ball num	J33 pin name	J33 Pin num	Description
		TRANSMIT		
SP6_TA_p	B21	P_TD0	A1	Port 6 Lane A non-inverting Transmit Data output.
SP6_TA_n	A21	N_TD0	B1	Port 6 Lane A inverting Transmit Data output.
SP6_TB_p	A19	P_TD1	A2	Port 6 Lane B non-inverting Transmit Data output.
SP6_TB_n	B19	N_TD1	B2	Port 6 Lane B inverting Transmit Data output.
SP6_TC_p	B17	P_TD2	A3	Port 6 Lane C non-inverting Transmit Data output.
SP6_TC_n	A17	N_TD2	B3	Port 6 Lane C inverting Transmit Data output.
SP6_TD_p	A15	P_TD3	A4	Port 6 Lane D non-inverting Transmit Data output.
SP6_TD_n	B15	N_TD4	B4	Port 6 Lane D inverting Transmit Data output.
		RECEIVE		
SP6_RA_p	D21	P_RD0	H10	Port 6 Lane A non-inverting Receive Data input.
SP6_RA_n	E21	N_RD0	G10	Port 6 Lane A inverting Receive Data input.
SP6_RB_p	E19	P_RD1	H9	Port 6 Lane B non-inverting Receive Data input.
SP6_RB_n	D19	N_RD1	G9	Port 6 Lane B inverting Receive Data input.

SP6_RC_p	D17	P_RD2	H8	Port 6 Lane C non-inverting Receive Data input.
SP6_RC_n	E17	N_RD2	G8	Port 6 Lane C inverting Receive Data input.
SP6_RD_p	E15	P_RD3	H7	Port 6 Lane D non-inverting Receive Data input.
SP6_RD_n	D15	N_RD4	G7	Port 6 Lane D inverting Receive Data input.

1.2.8 J34 – Power

Voltage Level	Pin Numbers
3.3V	A1 to A4, B1 to B4
ground	C1 to C4

1.2.9 J35 - Power

Voltage Level	Pin Numbers
5V	B1 to B4, C1 to C4
ground	A1 to A4

1.2.10 Configuration/Programming

Switches SW2 & SW4 control the Power-Down State of each Transmit and Receive Port. Changes are effected only following a reset of the Tsi578 device. Individual Serial RapidIO ports may be powered down to reduce the overall power consumption of the SRDP.

NOTE: Failure to follow this note may result in improper results from the board.

All configuration switch changes do not take effect until a HW_RST is applied to the Tsi578.

It should be noted that the Power-Down State may also be set externally via the J44 connector; however these switches must be set in the OFF position for J44 operation. The function of each switch is described below.

1.2.10.1 SW2 – Power Down Configuration Dipswitch

ON = closed = switch down = 0 = GND

OFF = open = switch up = 1 = 10k pull-up to 3.3V

Tsi578 pin name	Tsi578 ball num	SW2 switch num	J44 Pin num	Description
SP8_PWRDWN	Y1	1	18	Port 8 Tx and Rx power down control Controls the state all four lanes of Port 8 and Port 9. ON: Port 8 Powered Up, Port 9 controlled by SP9_PWRDWN OFF: Port 8 Powered Down, Port 9 Powered Down
SP9_PWRDWN	Y3	2	20	Port 9 Tx and Rx power down control Controls the state of Port 9. Note: Port 9 is never used when 4X mode is selected for Port 8 Serial Rapid IO MAC and it must be powered down. ON: Port 9 Powered Up OFF: Port 9 Powered Down
SP10_PWRDWN	Y4	3	22	Port 10 Tx and Rx power down control Controls the state all four lanes of Port 10 and Port 11. ON: Port 10 Powered Up, Port 11 controlled by SP11_PWRDWN OFF: Port 10 Powered Down, Port 11 Powered Down
SP11_PWRDWN	Y6	4	24	Port 11 Tx and Rx power down control Controls the state of Port 11. Note: Port 11 is never used when 4X mode is selected for Port 10 Serial Rapid IO MAC and it must be powered down. ON: Port 11 Powered Up OFF: Port 11 Powered Down
SP12_PWRDWN	AA2	5	26	Port 12 Tx and Rx power down control Controls the state all four lanes of Port 12 and Port 13. ON: Port 12 Powered Up, Port 13 controlled by SP13_PWRDWN OFF: Port 12 Powered Down, Port 13 Powered Down
SP13_PWRDWN	AA3	6	28	Port 13 Tx and Rx power down control Controls the state of Port 13. Note: Port 13 is never used when 4X mode is selected for Port 12 Serial Rapid IO MAC and it must be powered down. ON: Port 13 Powered Up OFF: Port 13 Powered Down
SP14_PWRDWN	W7	7	30	Port 14 Tx and Rx power down control Controls the state all four lanes of Port 14 and Port 15. ON: Port 14 Powered Up, Port 15 controlled by SP15_PWRDWN OFF: Port 14 Powered Down, Port 15 Powered Down

SP15_PWRDWN	Y8	8	32	Port 15 Tx and Rx power down control Controls the state of Port 15. Note: Port 15 is never used when 4X mode is selected for Port 14 Serial Rapid IO MAC and it must be powered down. ON: Port 15 Powered Up OFF: Port 15 Powered Down
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1.2.10.2 SW4 – Power Down Configuration Dipswitch

ON = closed = switch down = 0 = GND

OFF = open = switch up = 1 = 10k pull-up to 3.3V

Tsi578 pin name	Tsi578 ball num	SW4 switch num	J44 Pin num	Description
I ² C MA	AE22	1	2	Controls I ² C multi-byte peripheral addressing. ON: I ² C addressing is single byte OFF: I ² C addressing is multi-byte
SP1_PWRDWN	AF22	2	4	Port 1 Tx and Rx power down control Controls the state of Port 1. Note: Port 1 is never used when 4X mode is selected for Port 0 Serial Rapid IO MAC and it must be powered down. ON: Port 1 Powered Up OFF: Port 1 Powered Down
SP2_PWRDWN	AE23	3	6	Port 2 Tx and Rx power down control Controls the state all four lanes of Port 2 and Port 3. ON: Port 2 Powered Up, Port 3 controlled by SP3_PWRDWN OFF: Port 2 Powered Down, Port 3 Powered Down
SP3_PWRDWN	AF23	4	8	Port 3 Tx and Rx power down control Controls the state of Port 3. Note: Port 3 is never used when 4X mode is selected for Port 2 Serial Rapid IO MAC and it must be powered down. ON: Port 3 Powered Up OFF: Port 3 Powered Down
SP4_PWRDWN	W2	5	10	Port 4 Tx and Rx power down control Controls the state all four lanes of Port 4 and Port 5. ON: Port 4 Powered Up, Port 5 controlled by SP5_PWRDWN OFF: Port 4 Powered Down, Port 5 Powered Down
SP5_PWRDWN	W3	6	12	Port 5 Tx and Rx power down control Controls the state of Port 5. Note: Port 5 is never used when 4X mode is selected for Port 4 Serial Rapid IO MAC and it must be powered down. ON: Port 5 Powered Up OFF: Port 5 Powered Down

SP6_PWRDWN	W5	7	14	Port 6 Tx and Rx power down control Controls the state all four lanes of Port 6 and Port 7. ON: Port 6 Powered Up, Port 7 controlled by SP7_PWRDWN OFF: Port 6 Powered Down, Port 7 Powered Down
SP7_PWRDWN	W6	8	16	Port 7 Tx and Rx power down control Controls the state of Port 7. Note: Port 7 is never used when 4X mode is selected for Port 6 Serial Rapid IO MAC and it must be powered down. ON: Port 7 Powered Up OFF: Port 7 Powered Down

1.2.11 SW3 – Mode Select Programming Dipswitch

SW3 controls the operating Mode of each of the Ports. Changes are effected only following a reset of the Tsi578 device. It should be noted that the Mode may also be set externally via the J44 connector; however these switches must be set in the OFF position for J44 operation. The function of each switch is enumerated below.

ON = closed = switch down = 0 = GND

OFF = open = switch up = 1 = 10k pull-up to 3.3V

Tsi578 pin name	Tsi578 ball num	SW3 switch num	J44 Pin num	Description
SP0_MODESEL	AD22	1	1	PORT 0/1 Operating Mode This switch controls the Mode for Ports 0 and Port 1. ON: Port 0 operating in 4X mode (Port 1 not available) OFF: Ports 0 and 1 operating in 1X mode
SP2_MODESEL	AD23	2	5	PORT 2/3 Operating Mode This switch controls the Mode for Ports 2 and Port 3. ON: Port 2 operating in 4X mode (Port 3 not available) OFF: Ports 2 and 3 operating in 1X mode
SP4_MODESEL	AB1	3	9	PORT 4/5 Operating Mode This switch controls the Mode for Ports 4 and Port 5. ON: Port 4 operating in 4X mode (Port 5 not available) OFF: Ports 4 and 5 operating in 1X mode

SP6_MODESEL	AB3	4	13	<p>PORT 6/7 Operating Mode This switch controls the Mode for Ports 6 and Port 7.</p> <p>ON: Port 6 operating in 4X mode (Port 7 not available) OFF: Ports 6 and 7 operating in 1X mode</p>
SP8_MODESEL	AB4	5	17	<p>PORT 8/9 Operating Mode This switch controls the Mode for Ports 8 and Port 9.</p> <p>ON: Port 8 operating in 4X mode (Port 9 not available) OFF: Ports 8 and 9 operating in 1X mode</p>
SP10_MODESEL	AC3	6	21	<p>PORT 10/11 Operating Mode This switch controls the Mode for Ports 10 and Port 11.</p> <p>ON: Port 10 operating in 4X mode (Port 11 not available) OFF: Ports 10 and 11 operating in 1X mode</p>
SP12_MODESEL	AF3	7	25	<p>PORT 12/13 Operating Mode This switch controls the Mode for Ports 12 and Port 13.</p> <p>ON: Port 12 operating in 4X mode (Port 13 not available) OFF: Ports 12 and 13 operating in 1X mode</p>
SP14_MODESEL	AF4	8	29	<p>PORT 14/15 Operating Mode This switch controls the Mode for Ports 14 and Port 15.</p> <p>ON: Port 14 operating in 4X mode (Port 15 not available) OFF: Ports 14 and 15 operating in 1X mode</p>

1.2.12 SW5 – Speed Configuration Dipswitch

SW5 controls the Serial Port Transmit and Receive Operating Frequency, and selects the speed at which the port operates. The output data rate per lane is 10 times the selected input clock. Changes are effected only following a reset of the Tsi578 device. It should be noted that the Operating Frequency may also be set externally via the J44 connector; however these switches must be set in the OFF position for J44 operation. The function of each switch is enumerated below.

SW5-2	SW5-1	Data Rate Description
Speed 1	Speed 0	
OFF	OFF	Reserved
OFF	ON	3.125 Gbaud
ON	OFF	2.50 Gbaud
ON	ON	1.25 Gbaud

ON = closed = switch down = 0 = GND

OFF = open = switch up = 1 = 10k pull-up to 3.3V

Tsi578 pin name	Tsi578 ball num	SW5 switch num	J44 Pin num	Description
Tsi578_SPEED0	AC22	1	34	Serial port Tx and Rx operating frequency select bit 0
Tsi578_SPEED1	AC23	2	36	Serial port Tx and Rx operating frequency select bit 1

1.2.13 J44 – External Control Port

J44 provides a means to externally control and configure the Serial Rapid IO Evaluation Card. This interfaces provides control of the Tsi578 Power Down, Mode Select, Operating Frequency and Reset. This interface also provides an interface the 2-wire serial bus for each AMC card. A description of each signal is described in the table below.

NOTE: Failure to follow this note may result in improper results from the board.

All configuration signal changes do not take effect until a HW_RST is applied to the Tsi578.

Tsi578 pin name	Tsi578 ball num	switch num	J44 Pin num	Description
SP0_MODESEL	AD22	SW3-1	1	<p>SP0_MODESEL - PORT 0/1 Operating Mode</p> <p>This signal controls the Mode for Ports 0 and Port 1.</p> <p>0: Port 0 operating in 4X mode (Port 1 not available)</p> <p>1: Ports 0 and 1 operating in 1X mode</p> <p>Note: SW3-1 must be in the OFF position to use this external control signal.</p>
I ² C MA	AE22	SW4-1	2	<p>Controls I²C multi-byte peripheral addressing</p> <p>ON I²C addressing is single byte</p> <p>OFF I²C addressing is multi-byte</p> <p>The factory default position for SW4-1 is OFF. SW4-1 must be in the off position to permit boot loading from the EEPROM on power-up and to enable writing of data into the EEPROM.</p> <p>Note: SW4-1 must be in the OFF position to use this external control signal.</p>
Signal Ground			3	Signal Ground
SP1_PWRDWN	AF22	SW4-2	4	<p>SP1_PWRDWN - PORT 1 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 1. Note: Port 1 is never used when 4X mode is selected for Port 0 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 1 Powered Up</p> <p>1: Port 1 Powered Down.</p> <p>Note: SW4-2 must be in the OFF position to use this external control signal.</p>

Tsi578 pin name	Tsi578 ball num	switch num	J44 Pin num	Description
SP2_MODESEL	AD23	SW3-2	5	<p>SP2_MODESEL - PORT 2/3 Operating Mode This signal controls the Mode for Ports 2 and Port 3.</p> <p>0: Port 2 operating in 4X mode (Port 3 not available) 1: Ports 2 and 3 operating in 1X mode</p> <p>Note: SW3-2 must be in the OFF position to use this external control signal.</p>
SP2_PWRDWN	AE23	SW4-3	6	<p>SP2_PWRDN - PORT 2 Transmit & Receive Power Down Control. This signal controls the state all four lanes of Port 2 and Port 3.</p> <p>0: Port 2 Powered Up, Port 3 controlled by SP3_PWRDN 1: Port 2 Powered Down, Port 3 Powered Down</p> <p>Note: SW4-3 must be in the OFF position to use this external control signal.</p>
Signal Ground			7	Signal Ground
SP3_PWRDWN	AF23	SW4-4	8	<p>SP3_PWRDN - PORT 3 Transmit & Receive Power Down Control. This signal controls the state of Port 3. Note: Port 3 is never used when 4X mode is selected for Port 2 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 3 Powered Up 1: Port 3 Powered Down</p> <p>Note: SW4-4 must be in the OFF position to use this external control signal.</p>
SP4_MODESEL	AB1	SW3-3	9	<p>SP4_MODESEL - PORT 4/5 Operating Mode This signal controls the Mode for Ports 4 and Port 5.</p> <p>0: Port 4 operating in 4X mode (Port 5 not available) 1: Ports 4 and 5 operating in 1X mode</p> <p>Note: SW3-3 must be in the OFF position to use this external control signal.</p>

Tsi578 pin name	Tsi578 ball num	switch num	J44 Pin num	Description
SP4_PWRDWN	W2	SW4-5	10	<p>SP4_PWRDWN - PORT 4 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 4 and Port 5.</p> <p>0: Port 4 Powered Up, Port 5 controlled by SP5_PWRDWN 1: Port 4 Powered Down, Port 5 Powered Down</p> <p>Note: SW4-5 must be in the OFF position to use this external control signal.</p>
Signal Ground			11	Signal Ground
SP5_PWRDWN	W3	SW4-6	12	<p>SP5_PWRDWN - PORT 5 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 5. Note: Port 5 is never used when 4X mode is selected for Port 4 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 5 Powered Up 1: Port 5 Powered Down</p> <p>Note: SW4-6 must be in the OFF position to use this external control signal.</p>
SP6_MODESEL	AB3	SW3-4	13	<p>SP6_MODESEL - PORT 6/7 Operating Mode</p> <p>This signal controls the Mode for Ports 6 and Port 7.</p> <p>0: Port 6 operating in 4X mode (Port 7 not available) 1: Ports 6 and 7 operating in 1X mode</p> <p>Note: SW3-4 must be in the OFF position to use this external control signal.</p>
SP6_PWRDWN	W5	SW4-7	14	<p>SP6_PWRDWN - PORT 6 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 6 and Port 7.</p> <p>0: Port 6 Powered Up, Port 7 controlled by SP7_PWRDWN 1: Port 6 Powered Down, Port 7 Powered Down</p> <p>Note: SW4-7 must be in the OFF position to use this external control signal.</p>

Tsi578 pin name	Tsi578 ball num	switch num	J44 Pin num	Description
Signal Ground			15	Signal Ground
SP7_PWRDWN	W6	SW4-8	16	<p>SP7_PWRDN - PORT 7 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 7. Note: Port 7 is never used when 4X mode is selected for Port 6 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 7 Powered Up 1: Port 7 Powered Down</p> <p>Note: SW4-8 must be in the OFF position to use this external control signal.</p>
SP8_MODESEL	AB4	SW3-5	17	<p>SP8_MODESEL - PORT 8/9 Operating Mode</p> <p>This signal controls the Mode for Ports 8 and Port 9.</p> <p>0: Port 8 operating in 4X mode (Port 9 not available) 1: Ports 8 and 9 operating in 1X mode</p> <p>Note: SW3-5 must be in the OFF position to use this external control signal.</p>
SP8_PWRDWN	Y1	SW2-1	18	<p>SP8_PWRDN - PORT 8 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 8 and Port 9.</p> <p>0: Port 8 Powered Up, Port 9 controlled by SP9_PWRDN 1: Port 8 Powered Down, Port 9 Powered Down</p> <p>Note: SW2-1 must be in the OFF position to use this external control signal.</p>
Signal Ground			19	Signal Ground

Tsi578 pin name	Tsi578 ball num	switch num	J44 Pin num	Description
SP9_PWRDWN	Y3	SW2-2	20	<p>SP9_PWRDN - PORT 9 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 9. Note: Port 9 is never used when 4X mode is selected for Port 8 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 9 Powered Up 1: Port 9 Powered Down</p> <p>Note: SW2-2 must be in the OFF position to use this external control signal.</p>
SP10_MODESEL	AC3	SW3-6	21	<p>SP10_MODESEL - PORT 10/11 Operating Mode</p> <p>This signal controls the Mode for Ports 10 and Port 11.</p> <p>0: Port 10 operating in 4X mode (Port 11 not available) 1: Ports 10 and 11 operating in 1X mode</p> <p>Note: SW3-6 must be in the OFF position to use this external control signal.</p>
SP10_PWRDWN	Y4	SW2-3	22	<p>SP10_PWRDN - PORT 10 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 10 and Port 11.</p> <p>0: Port 10 Powered Up, Port 11 controlled by SP11_PWRDN 1: Port 10 Powered Down, Port 11 Powered Down</p> <p>Note: SW2-3 must be in the OFF position to use this external control signal.</p>
Signal Ground			23	Signal Ground

Tsi578 pin name	Tsi578 ball num	switch num	J44 Pin num	Description
SP11_PWRDWN	Y6	SW2-4	24	<p>SP11_PWRDN - PORT 11 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 11. Note: Port 11 is never used when 4X mode is selected for Port 10 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 11 Powered Up 1: Port 11 Powered Down</p> <p>Note: SW2-4 must be in the OFF position to use this external control signal.</p>
SP12_MODESEL	AF3	SW3-7	25	<p>SP12_MODESEL - PORT 12/13 Operating Mode</p> <p>This signal controls the Mode for Ports 12 and Port 13.</p> <p>0: Port 12 operating in 4X mode (Port 13 not available) 1: Ports 12 and 13 operating in 1X mode</p> <p>Note: SW3-7 must be in the OFF position to use this external control signal.</p>
SP12_PWRDWN	AA2	SW2-5	26	<p>SP12_PWRDN - PORT 12 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 12 and Port 13.</p> <p>0: Port 12 Powered Up, Port 13 controlled by SP13_PWRDN 1: Port 12 Powered Down, Port 13 Powered Down</p> <p>Note: SW2-5 must be in the OFF position to use this external control signal.</p>
Signal Ground			27	Signal Ground

Tsi578 pin name	Tsi578 ball num	switch num	J44 Pin num	Description
SP13_PWRDWN	AA3	SW2-6	28	<p>SP13_PWRDN - PORT 13 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 13. Note: Port 13 is never used when 4X mode is selected for Port 12 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 13 Powered Up 1: Port 13 Powered Down</p> <p>Note: SW2-6 must be in the OFF position to use this external control signal.</p>
SP14_MODESEL	AF4	SW3-8	29	<p>SP14_MODESEL - PORT 14/15 Operating Mode</p> <p>This signal controls the Mode for Ports 14 and Port 15.</p> <p>0: Port 14 operating in 4X mode (Port 15 not available) 1: Ports 14 and 15 operating in 1X mode</p> <p>Note: SW3-8 must be in the OFF position to use this external control signal.</p>
SP14_PWRDWN	W7	SW2-7	30	<p>SP14_PWRDN - PORT 14 Transmit & Receive Power Down Control.</p> <p>This signal controls the state all four lanes of Port 14 and Port 15.</p> <p>0: Port 14 Powered Up, Port 15 controlled by SP15_PWRDN 1: Port 14 Powered Down, Port 15 Powered Down</p> <p>Note: SW2-7 must be in the OFF position to use this external control signal.</p>
HARD_RST_B	AF2		31	<p>Active low Tsi578 Hardware Reset. Must be held low for a minimum of 1 ms.</p>

Tsi578 pin name	Tsi578 ball num	switch num	J44 Pin num	Description
SP15_PWRDWN	Y8	SW2-8	32	<p>SP15_PWRDWN - PORT 15 Transmit & Receive Power Down Control.</p> <p>This signal controls the state of Port 15. Note: Port 15 is never used when 4X mode is selected for Port 14 Serial Rapid IO MAC and it must be powered down.</p> <p>0: Port 15 Powered Up 1: Port 15 Powered Down</p> <p>Note: SW2-8 must be in the OFF position to use this external control signal.</p>
n/a	n/a	n/a	33	AMC 0, IPMB-L Clock. This signal is the IPMB-L I ² C Clock for AMC Port 0.
Tsi578_SPEED0	AC22	SW5-1	34	<p>See Tsi578_SPEED0 (pin 36)</p> <p>Note: SW5-1 must be in the OFF position to use this external control signal.</p>
n/a	n/a	n/a	35	AMC 0, IPMB-L Data. This signal is the IPMB-L I ² C Data for AMC Port 0.
Tsi578_SPEED1	AC23	SW5-2	36	<p>Serial Port Transmit and Receive Operating Frequency. In conjunction with Tsi578_SPEED0 selects the speed at which the ports operate. The output data rate per lane is 10 times the selected input clock. Changes are effected only following a reset of the Tsi578 device. The function of each signal is enumerated below.</p> <p>Tsi578_SPEED1, Tsi578_SPEED0 See SW5 table for corresponding data rates.</p> <p>Note: SW5-2 must be in the OFF position to use this external control signal.</p>
n/a	n/a	n/a	37	AMC 1, IPMB-L Clock. This signal is the IPMB-L I ² C Clock for AMC Port 1.
n/a	n/a	n/a	38	AMC 2, IPMB-L Clock. This signal is the IPMB-L I ² C Clock for AMC Port 2.
n/a	n/a	n/a	39	AMC 1, IPMB-L Data. This signal is the IPMB-L I ² C Data for AMC Port 1.
n/a	n/a	n/a	40	AMC 2, IPMB-L Data. This signal is the IPMB-L I ² C Data for AMC Port 2.

1.2.14 JTAG Headers

The SRDP supports JTAG programming of the Tsi578 through the JTAG connector J45 as well as through peripheral devices on AMC cards through the AMC JTAG connector J46.

1.2.14.1 J45 - Tsi578 JTAG Header

Tsi578 pin name	Tsi578 ball num	J45 Pin num	Description
TDO	AD25	1	Tsi578 TDO
		2	No connect
TDI	AD26	3	Tsi578 TDI
TRST_B	AE26	4	Tsi578 TRST
		5	No connect
		6	3.3V
TCK	AF26	7	Tsi578 TCK
		8	No connect
TMS	AC26	9	Tsi578 TMS
		10	No connect
		11	No connect
		12	GND
		13	No connect
		14	No connect
		15	No connect
		16	GND

1.2.14.2 J46 - AMC JTAG Header

AMC Header pin name	AMC Pin num	J46 Pin num	Description
AMC_CHN1	J39-B169	1	AMC Interface 0 pin B169
		2	No connect
AMC_CHN4	J41-B169	3	AMC Interface 2 pin B169
AMC_TRST	B167	4	TRST for AMC interface 0 to 2
		5	No connect
		6	3.3V
AMC_TCK	B165	7	TCK for AMC interface 0 to 2
		8	No connect
AMC_TMS	B166	9	TMS for AMC interface 0 to 2
		10	No connect
		11	No connect
		12	GND
		13	No connect
		14	No connect
		15	No connect
		16	GND

1.2.15 J38 - External Status Port

J38 provides a means for external access to the system status signals. The table below describes the function of each pin.

J38 PIN	SIGNAL	DESCRIPTION
1	Not used	
2	Tsi578_INT	Tsi578 Interrupt signal.
3	Not used	
4	Tsi578_SW_RST	Tsi578 Software reset. This signal is asserted when a Rapid IO port valid reset request on a Rapid IO link. If self reset is not selected, this signal remains asserted until the reset request is cleared from the status registers. If self reset is selected, this pin remains asserted until the self reset is complete. If the Tsi578 is reset from the HARD_RESET_b pin, this pin is de-asserted and remains de-asserted after HARD_RESET_b is released.
5	Not used	
6	EN_1V2_N	Active low signal indicating that both the 12V and 3.3V power rails are active and within specified limits. Note: this signal is at 5V CMOS levels.
7	Not used	
8	1V2_GOOD	Active high signal indicating that the 1.2V power is active and within specified limits. Note: this signal is at 5V CMOS levels.
9	Not used	
10	3V3_GOOD	Active high signal indicating that the 3.3V power is active and within specified limits. Note: this signal is at 5V CMOS levels.
11	Not used	
12	Not used	
13	Not used	
14	Not used	
15	Signal Ground	
16	SYS_RESET_N	Active low System Reset. This signal is active for a minimum of 1 ms. Note: this signal is at 3.3V CMOS levels.

2.0 SRDP HARDWARE DESIGN & ARCHITECTURE

2.1 General Description

Some of the features and characteristics of the SRDP are:

- 80 Gbits/s aggregate bandwidth
- More processing power-per-watt via distributed CPUs
- Highly configurable
- Low power consumption
- Compliant to RapidIO Specification (Revision 1.3)

Typical Applications for Serial RIO

- System level solutions with Qos demands
- Mesh networking, wired or wireless
- Multiprocessor systems
- ASIC/SOC/IP development
- Deterministic board to board solutions
- Low overhead SMP implementations

2.2 Physical Specifications

Board Size.....	302 x 322mm
Power Requirements.....	Standard ATX Supply
Operating Temperature.....	0° to 70°C
Standards Compliance.....	RapidIO Specifications (Rev 1.2)
Weight.....	1.5Kg
RoHS.....	Compliant

Figure 3 below is a block diagram of the Tsi578 switch and how it interfaces to the associated connectors supported on the SRDP board.

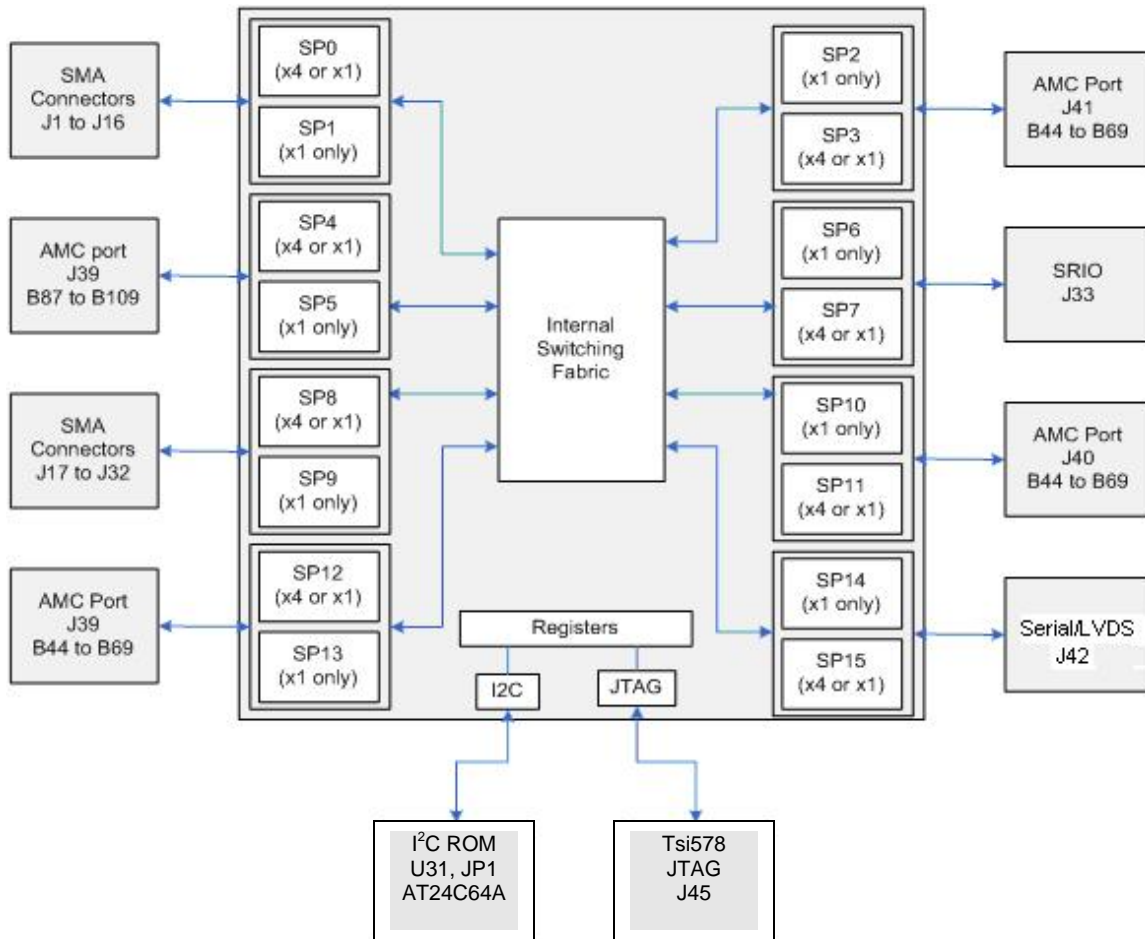


Figure 3 – Block Diagram

2.3 Hardware Configuration

The SRDP has user configurable options that include:

- Port Speed
- External EEPROM access
- Serial RapidIO port mode select
- Power Down options.

2.3.1.1 S_CLK1

Selection jumper JP5 must be installed if an external clock generator is to be used. The external clock generator is connected to SMA J55 and provides the input source for Tsi578 S_CLK1. If JP5 is not installed then the on-board clock circuitry provides the clocking signal. JP5 not installed is the factory default.

NOTE: Failure to follow this note may result in improper results from the board.

The Tsi578 S_CLK1 operates at 156.25MHz. The signal source should be at LVCMOS/LVTTL levels.

Frequency Selection Jumper JP7 must be properly set for either internal or external clock use. Refer to the table below for the correct configuration.

JP6	JP7	Frequency
Not installed	Not installed	Not a valid operating frequency
Installed	Installed	156.25 MHz Factory default
Installed	Not installed	External clock source

JP7 Selection Jumper Table

Output Enable Jumper JP4 enables the Tsi578 S_CLK1 outputs from the on-board clock generator to the SMA connectors J53 and J54 as well as the test points on connector JP3. These signals can be monitored with an oscilloscope connected to SMA connectors J53 and J54 or from a logic analyzer connected to JP3. The signal levels are LVPECL. These signals are only viewable when Jumper JP4 is installed. JP4 installed is the factory default.

The table below identifies the Tsi578 S_CLK1 pin assignments on connector JP3.

Pin Name	Signal Name
1	Tsi578 S_CLK1_p
2	Signal Ground
3	Tsi578 S_CLK1_n

JP3 Test Connector Table

2.3.2 Port Speed Selection – SW5

Dipswitch SW5 determines the Port Speed selected. This switch controls the Serial RapidIO ports Transmit and Receive data rates.

The Serial RapidIO ports use source-clocked transmission which is embedded in the data stream using 8B/10B encoding. The Tsi578 decodes the embedded clock and generates a separate clock to transmit its own data.

The Tsi578 supports three difference signal rates that are generated from the two clock sources. The data rate is determined by the setting of the Serial RapidIO Port Speed Selection Dipswitch SW5. Refer to section 1.2.12 for details on the SW5 dipswitch settings.

NOTE: Failure to follow this note may result in improper results from the board.

The Serial RapidIO specification requires the transmit and receive signals to be at the same rate.

Additionally, the difference in speed between the transmit and receive clocks are +/- 200 parts per million maximum.

2.3.3 I²C External EEPROM Enable Jumper – JP1

With jumper JP1 installed, the Tsi578 can access the external EEPROM at boot-up after the chip receives a reset from the I²C interface. If the jumper is not installed, I²C register information must come from an external JTAG connection. JP1 installed is the factory default.

NOTE: Failure to follow this note may result in improper results from the board.

The EEPROM (U31) comes preloaded from the factory with initialization code for the Tsi578 device.

Refer to Appendix B for complete details.

2.3.3.1 I²C Interface

When the Tsi578 comes out of reset, the I²C Interface is responsible for performing automatic reads from an externally attached EEPROM device in order to load the initial configuration of the device. The Tsi578 I²C Interface issues an EEPROM reset immediately following the chip hardware reset (HARD_RST_b). The purpose of the EEPROM reset is to re-synchronize the serial EEPROM with the I²C Interface, after the interface has been reset.

The Tsi578 I²C Interface generates an EEPROM reset by pulling the SDA signal (I²C serial data line) high while putting out a sequence of nine pulses on SCLK signal (I²C serial clock). The nine SCLK pulses clear the I²C transaction that was in progress prior to the reset and provides one or more NACK signals. Following the ninth pulse, both the SDA signal and the SCLK signal are left high.

2.4 Logic Analyzer Test Connectors (J47 to J52)

These connectors provide a convenient logic analyzer interface to the following Serial RapidIO ports:

- Tsi578 Port 6: Serial/HIP Interface (J47)
- Tsi578 Port 12: AMC_0 (J48)
- Tsi578 Port 4: AMC_0 (J49)
- Tsi578 Port 10: AMC_1 (J50)
- Tsi578 Port 2: AMC_2 (J51)
- Tsi578 Port 14: Serial/LVDS (J52)

These industry standard interfaces provide the user a direct connection to standard logic analyzer compression-type probes. The table below shows the signal assignment on each interface.

The signals available are listed in the table below.

Pin Number	Signal	Pin Number	Signal
1	RA_p	2	GND
3	RA_n	4	TA_p
5	GND	6	TA_n
7	RB_p	8	GND
9	RB_n	10	TB_p
11	GND	12	TB_n
13	RC_p	14	GND
15	RC_n	16	TC_p
17	GND	18	TC_n
19	RD_p	20	GND
21	RD_n	22	TD_p
23	GND	24	TD_n

3.0 SRDP CONNECTIVITY & CONFIGURATION

This section contains general set-up information about the SRDP board. Refer to Figure 1 for jumper and switch locations.

3.1 Default Settings

Table 1 below defines the recommended default Jumper settings for the SRDP. Table 2 shows the recommended default Switch settings for the SRDP.

Settings of the jumpers and switches as shipped from STx may not reflect this set-up. Therefore it is recommended that you review these settings prior to powering the board up.

JUMPER	DESCRIPTION	DEFAULT SETTING
JP1	External EEPROM Access Jumper	Installed (enabled)
JP2	ATX Power Enable Jumper	Installed (enabled)
JP3	S_CLK1 Test Connector	N/A
JP4	S_CLK1 Test Clock Output Enable Jumper	Installed (enabled)
JP5	S_CLK1 Source Selection Jumper	Not installed
JP6	S_CLK1 On-board Source Frequency Selection Jumper	Installed (156.25MHz)
JP7	S_CLK1 On-board Source Frequency Selection Jumper	Installed (156.25MHz)

Table 1 – Default Jumper Settings

DIP-SWITCH	DESCRIPTION	DEFAULT SETTING
SW1	Manual System Reset	Pushbutton (N/A)
SW2	Serial RapidIO Port Power Down Configurations	ON (Powered Up)
SW3	Serial RapidIO Port Mode Select	ON (All ports in 4x mode)
SW4	Serial RapidIO Port Power Down Configurations	OFF (Powered Down)
SW5	Serial RapidIO Port Speed Selection	ON (1.25 Gbits/s bit rate)

Table 2 – Default Switch Settings

Appendix A – Schematic

The schematic for the SRDP is on the accompanying CD supplied with the board.

Appendix B – EEPROM Programming

NOTE:	Failure to follow this note may result in improper results from the board. The information contained in this section is for use on boards that incorporate the Tundra Semiconductor part Tsi578-10GCLYZ1 only.
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The information in this appendix should be followed if you need to append the factory pre-loaded file currently residing in the EEPROM (U31). The firmware currently loaded into the EEPROM contains initialization code for the Tsi578 and should not be deleted.

You will first need to contact Tundra Semiconductor for a copy of their programming software tool called *JTUNDRA.exe*. You can contact Tundra at www.tundra.com or by calling 800-267-7231. This JTAG software is used in conjunction with a Wiggler/COP debugging tool that can be purchased from Macraigor Systems. You can contact Macraigor at www.macraigor.com or by calling 206-855-9269.

In addition to the JTUNDRA program and Wiggler, there are two (2) other required files. These are located on the CD supplied by STx with your board.

The first one is a text file called *Tsi578 SRDP EEPROM instructions.txt* which contains the necessary information on how to append the existing contents of the EEPROM. The second file is a text script file that will execute the program. It is called *tx_done_i2c_srdp.txt*.

The text files are shown below.

Tsi578 SRDP EEPROM instructions.txt

Process for appending user register writes to the existing contents of the EEPROM:

1/ The EEPROM is formatted into 3 distinct sections (see also section 7.8.7 of the Tsi578 user manual):

- 0x0000 0xaaaa / the hex number of registers that will be affected by the boot load
- 0x0002 0xFFFF / this field is always 0xFFFF
- 0x0004 0xFFFF / this field is always 0xFFFF
- 0x0006 0xFFFF / this field is always 0xFFFF
- 0x0008 0xyyyy / this is the beginning of the boot load memory space. It contains the address of the first register to be initialized by the EEPROM boot load.

2/ This is an image of the contents that are currently required in the EEPROM and must be present at all times. Sixty-five registers are modified by the boot load.

```
0x0000 0041FFFF FFFFFFFF 0001e00c 00000021
0x0010 0001e00c 00000029 0001e04c 00000021
0x0020 0001e04c 00000029 0001e08c 00000021
0x0030 0001e08c 00000029 0001e0cc 00000021
0x0040 0001e0cc 00000029 0001e20c 00000021
0x0050 0001e20c 00000029 0001e24c 00000021
0x0060 0001e24c 00000029 0001e28c 00000021
0x0070 0001e28c 00000029 0001e2cc 00000021
0x0080 0001e2cc 00000029 0001e40c 00000021
0x0090 0001e40c 00000029 0001e44c 00000021
0x00a0 0001e44c 00000029 0001e48c 00000021
0x00b0 0001e48c 00000029 0001e4cc 00000021
0x00c0 0001e4c0 00000029 0001e60c 00000021
0x00d0 0001e60c 00000029 0001e64c 00000021
0x00e0 0001e64c 00000029 0001e68c 00000021
0x00f0 0001e68c 00000029 0001e6cc 00000021
0x0100 0001e6cc 00000029 0001e80c 00000021
0x0110 0001e80c 00000029 0001e84c 00000021
0x0120 0001e84c 00000029 0001e88c 00000021
0x0130 0001e88c 00000029 0001e8cc 00000021
0x0140 0001e8cc 00000029 0001ea0c 00000021
0x0150 0001ea0c 00000029 0001ea4c 00000021
0x0160 0001ea4c 00000029 0001ea8c 00000021
0x0170 0001ea8c 00000029 0001eacc 00000021
0x0180 0001eacc 00000029 0001ec0c 00000021
0x0190 0001ec0c 00000029 0001ec4c 00000021
0x01a0 0001ec4c 00000029 0001ec8c 00000021
0x01b0 0001ec8c 00000029 0001eccc 00000021
0x01c0 0001eccc 00000029 0001ee0c 00000021
0x01d0 0001ee0c 00000029 0001ee4c 00000021
0x01e0 0001ee4c 00000029 0001ee8c 00000021
0x01f0 0001ee8c 00000029 0001eccc 00000021
0x0200 0001eccc 00000029 00000008 12345678
```

3/ To add more register writes to the end of the required boot load, append the address of the destination register and the data to be written into that register to the end of the current contents so that it looks like the memory dump below.

(This example writes to the look-up tables of ports 3 and 5.

It maps device ID 02 on port 3 and device ID 13 on port 5 for packet routing between each other.)

Append the new register addresses and their data beginning at address 0x00D0. In this case, 4 register writes are required to take place. Then change the word at 0x0000, incrementing it by the number of additional registers are going to be written. In this case the value changes from 0x0041 to 0x0045.

```
0x0000 0x0045FFFF FFFFFFFF 0001e00c 00000021 // change register write count
at
0x0010 0x0001e00c 00000029 0001e04c 00000021 // location 0x0000 from 0041 to
0045
0x0020 0x0001e04c 00000029 0001e08c 00000021 // to add 4 registers to the boot
load.
.....
0x01e0 0x0001ee4c 00000029 0001ee8c 00000021
0x01f0 0x0001ee8c 00000029 0001e0cc 00000021
0x0200 0x0001e0cc 00000029 00000008 12345678 // end of required data
0x0210 0x00011370 00000013 00011374 00000005 // beginning of user data
0x0220 0x00011570 00000002 00011574 00000003 // current end of user data
```

In script form, or command line format for use with the Tundra JTAG software, JTUNDRA.EXE, the commands to append additional user register writes would look as shown below:

```
w 1d114 0x00011370
w 1d10c 0xc4000210
w 1d114 0x00000013
w 1d10c 0xc4000214

w 1d114 0x00011374
w 1d10c 0xc4000218
w 1d114 0x00000005
w 1d10c 0xc400021C

w 1d114 0x00011570
w 1d10c 0xc4000220
w 1d114 0x00000002
w 1d10c 0xc4000224

w 1d114 0x00011574
w 1d10c 0xc4000228
w 1d114 0x00000003
w 1d10c 0xc400022C
//
```

tx_done i2c srdp.txt

//Setup software for the 578
ac Tsi578

//Switch 0 i2c setup
i 0

//Set number of registers to load
w 1d114 0x0041FFFF // num registers
w 1d10c 0xc4000000
w 1d114 0xFFFFFFFF
w 1d10c 0xc4000004

//1

//Toggle tx_done on all serdes
w 1d114 0x0001e00c //P0, Lane A
w 1d10c 0xc4000008
w 1d114 0x00000021
w 1d10c 0xc400000c

//2

w 1d114 0x0001e00c
w 1d10c 0xc4000010
w 1d114 0x00000029
w 1d10c 0xc4000014

//3

w 1d114 0x0001e04c //P0, Lane B
w 1d10c 0xc4000018
w 1d114 0x00000021
w 1d10c 0xc400001c

//4

w 1d114 0x0001e04c
w 1d10c 0xc4000020
w 1d114 0x00000029
w 1d10c 0xc4000024

//5

w 1d114 0x0001e08c //P0, Lane C
w 1d10c 0xc4000028
w 1d114 0x00000021
w 1d10c 0xc400002c

//6

w 1d114 0x0001e08c
w 1d10c 0xc4000030
w 1d114 0x00000029
w 1d10c 0xc4000034

//7

w 1d114 0x0001e0cc //P0, Lane D
w 1d10c 0xc4000038
w 1d114 0x00000021
w 1d10c 0xc400003c

//8

w 1d114 0x0001e0cc

w 1d10c 0xc4000040
w 1d114 0x00000029
w 1d10c 0xc4000044
//9
w 1d114 0x0001e20c //P2, Lane A
w 1d10c 0xc4000048
w 1d114 0x00000021
w 1d10c 0xc400004c
//A
w 1d114 0x0001e20c
w 1d10c 0xc4000050
w 1d114 0x00000029
w 1d10c 0xc4000054
//B
w 1d114 0x0001e24c //P2, Lane B
w 1d10c 0xc4000058
w 1d114 0x00000021
w 1d10c 0xc400005c
//C
w 1d114 0x0001e24c
w 1d10c 0xc4000060
w 1d114 0x00000029
w 1d10c 0xc4000064
//D
w 1d114 0x0001e28c //P2, Lane C
w 1d10c 0xc4000068
w 1d114 0x00000021
w 1d10c 0xc400006c
//E
w 1d114 0x0001e28c
w 1d10c 0xc4000070
w 1d114 0x00000029
w 1d10c 0xc4000074
//F
w 1d114 0x0001e2cc //P2, Lane D
w 1d10c 0xc4000078
w 1d114 0x00000021
w 1d10c 0xc400007c
//10
w 1d114 0x0001e2cc
w 1d10c 0xc4000080
w 1d114 0x00000029
w 1d10c 0xc4000084
//11
w 1d114 0x0001e40c //P4, Lane A
w 1d10c 0xc4000088
w 1d114 0x00000021
w 1d10c 0xc400008c
//12
w 1d114 0x0001e40c
w 1d10c 0xc4000090

w 1d114 0x00000029
w 1d10c 0xc4000094
//13
w 1d114 0x0001e44c //P4, Lane B
w 1d10c 0xc4000098
w 1d114 0x00000021
w 1d10c 0xc400009c
//14
w 1d114 0x0001e44c
w 1d10c 0xc40000a0
w 1d114 0x00000029
w 1d10c 0xc40000a4
//15
w 1d114 0x0001e48c //P4, Lane C
w 1d10c 0xc40000a8
w 1d114 0x00000021
w 1d10c 0xc40000ac
//16
w 1d114 0x0001e48c
w 1d10c 0xc40000b0
w 1d114 0x00000029
w 1d10c 0xc40000b4
//17
w 1d114 0x0001e4cc //P4, Lane D
w 1d10c 0xc40000b8
w 1d114 0x00000021
w 1d10c 0xc40000bc
//18
w 1d114 0x0001e4c0
w 1d10c 0xc40000c8
w 1d114 0x00000029
w 1d10c 0xc40000c4
//19
w 1d114 0x0001e60c //P6, Lane A
w 1d10c 0xc40000c8
w 1d114 0x00000021
w 1d10c 0xc40000cc
//1A
w 1d114 0x0001e60c
w 1d10c 0xc40000d0
w 1d114 0x00000029
w 1d10c 0xc40000d4
//1B
w 1d114 0x0001e64c //P6, Lane B
w 1d10c 0xc40000d8
w 1d114 0x00000021
w 1d10c 0xc40000dc
//1C
w 1d114 0x0001e64c
w 1d10c 0xc40000e0
w 1d114 0x00000029

w 1d10c 0xc40000e4
//1D
w 1d114 0x0001e68c //P6, Lane C
w 1d10c 0xc40000e8
w 1d114 0x00000021
w 1d10c 0xc40000ec
//1E
w 1d114 0x0001e68c
w 1d10c 0xc40000f0
w 1d114 0x00000029
w 1d10c 0xc40000f4
//1F
w 1d114 0x0001e6cc //P6, Lane D
w 1d10c 0xc40000f8
w 1d114 0x00000021
w 1d10c 0xc40000fc
//20
w 1d114 0x0001e6cc
w 1d10c 0xc4000100
w 1d114 0x00000029
w 1d10c 0xc4000104
//21
w 1d114 0x0001e80c //P8, Lane A
w 1d10c 0xc4000108
w 1d114 0x00000021
w 1d10c 0xc400010c
//22
w 1d114 0x0001e80c
w 1d10c 0xc4000110
w 1d114 0x00000029
w 1d10c 0xc4000114
//23
w 1d114 0x0001e84c //P8, Lane B
w 1d10c 0xc4000118
w 1d114 0x00000021
w 1d10c 0xc400011c
//24
w 1d114 0x0001e84c
w 1d10c 0xc4000120
w 1d114 0x00000029
w 1d10c 0xc4000124
//25
w 1d114 0x0001e88c //P8, Lane C
w 1d10c 0xc4000128
w 1d114 0x00000021
w 1d10c 0xc400012c
//26
w 1d114 0x0001e88c
w 1d10c 0xc4000130
w 1d114 0x00000029
w 1d10c 0xc4000134

//27
w 1d114 0x0001e8cc //P8, Lane D
w 1d10c 0xc4000138
w 1d114 0x00000021
w 1d10c 0xc400013c
//28
w 1d114 0x0001e8cc
w 1d10c 0xc4000140
w 1d114 0x00000029
w 1d10c 0xc4000144
//29
w 1d114 0x0001ea0c //P10, Lane A
w 1d10c 0xc4000148
w 1d114 0x00000021
w 1d10c 0xc400014c
//2A
w 1d114 0x0001ea0c
w 1d10c 0xc4000150
w 1d114 0x00000029
w 1d10c 0xc4000154
//2B
w 1d114 0x0001ea4c //P10, Lane B
w 1d10c 0xc4000158
w 1d114 0x00000021
w 1d10c 0xc400015c
//2C
w 1d114 0x0001ea4c
w 1d10c 0xc4000160
w 1d114 0x00000029
w 1d10c 0xc4000164
//2D
w 1d114 0x0001ea8c //P10, Lane C
w 1d10c 0xc4000168
w 1d114 0x00000021
w 1d10c 0xc400016c
//2E
w 1d114 0x0001ea8c
w 1d10c 0xc4000170
w 1d114 0x00000029
w 1d10c 0xc4000174
//2F
w 1d114 0x0001eacc //P10, Lane D
w 1d10c 0xc4000178
w 1d114 0x00000021
w 1d10c 0xc400017c
//30
w 1d114 0x0001eacc
w 1d10c 0xc4000180
w 1d114 0x00000029
w 1d10c 0xc4000184
//31

w 1d114 0x0001ec0c //P12, Lane A
w 1d10c 0xc4000188
w 1d114 0x00000021
w 1d10c 0xc400018c
//32
w 1d114 0x0001ec0c
w 1d10c 0xc4000190
w 1d114 0x00000029
w 1d10c 0xc4000194
//33
w 1d114 0x0001ec4c //P12, Lane B
w 1d10c 0xc4000198
w 1d114 0x00000021
w 1d10c 0xc400019c
//34
w 1d114 0x0001ec4c
w 1d10c 0xc40001a0
w 1d114 0x00000029
w 1d10c 0xc40001a4
//35
w 1d114 0x0001ec8c //P12, Lane C
w 1d10c 0xc40001a8
w 1d114 0x00000021
w 1d10c 0xc40001ac
//36
w 1d114 0x0001ec8c
w 1d10c 0xc40001b0
w 1d114 0x00000029
w 1d10c 0xc40001b4
//37
w 1d114 0x0001eccc //P12, Lane D
w 1d10c 0xc40001b8
w 1d114 0x00000021
w 1d10c 0xc40001bc
//38
w 1d114 0x0001eccc
w 1d10c 0xc40001c0
w 1d114 0x00000029
w 1d10c 0xc40001c4
//39
w 1d114 0x0001ee0c //P14, Lane A
w 1d10c 0xc40001c8
w 1d114 0x00000021
w 1d10c 0xc40001cc
//3A
w 1d114 0x0001ee0c
w 1d10c 0xc40001d0
w 1d114 0x00000029
w 1d10c 0xc40001d4
//3B
w 1d114 0x0001ee4c //P14, Lane B

```
w 1d10c 0xc40001d8
w 1d114 0x00000021
w 1d10c 0xc40001dc
//3C
w 1d114 0x0001ee4c
w 1d10c 0xc40001e0
w 1d114 0x00000029
w 1d10c 0xc40001e4
//3D
w 1d114 0x0001ee8c //P14, Lane C
w 1d10c 0xc40001e8
w 1d114 0x00000021
w 1d10c 0xc40001ec
//3E
w 1d114 0x0001ee8c
w 1d10c 0xc40001f0
w 1d114 0x00000029
w 1d10c 0xc40001f4
//3F
w 1d114 0x0001eccc //P14, Lane D
w 1d10c 0xc40001f8
w 1d114 0x00000021
w 1d10c 0xc40001fc
//40
w 1d114 0x0001eccc
w 1d10c 0xc4000200
w 1d114 0x00000029
w 1d10c 0xc4000204
//41
w 1d114 0x00000008 //Set Assembly ID
w 1d10c 0xc4000208
w 1d114 0x12345678
w 1d10c 0xc400020c
```