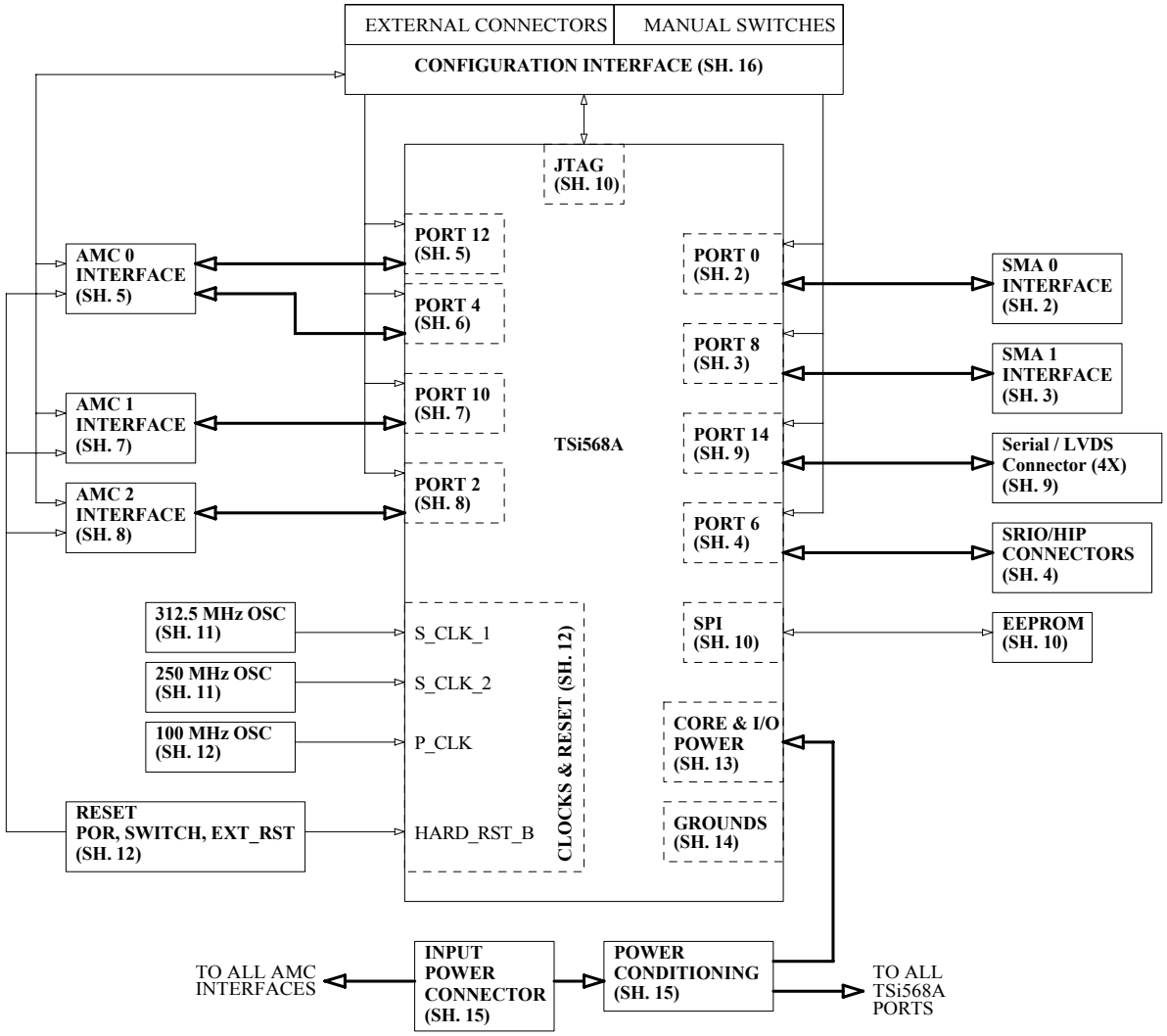

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SHEET 3	SRIO SMA INTERFACE 1, TSi568A Port 8
SHEET 4	SRIO HIP INTERFACE 0, TSi568A Port 6
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SHEET 10	TSI568A JTAG AND CONFIGURATION PORTS
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Silicon Turnkey Express, a division of RPC Electronics Inc.
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Highland Heights, Ohio 44143
www.siliconttx.com

Title: **SRDP**

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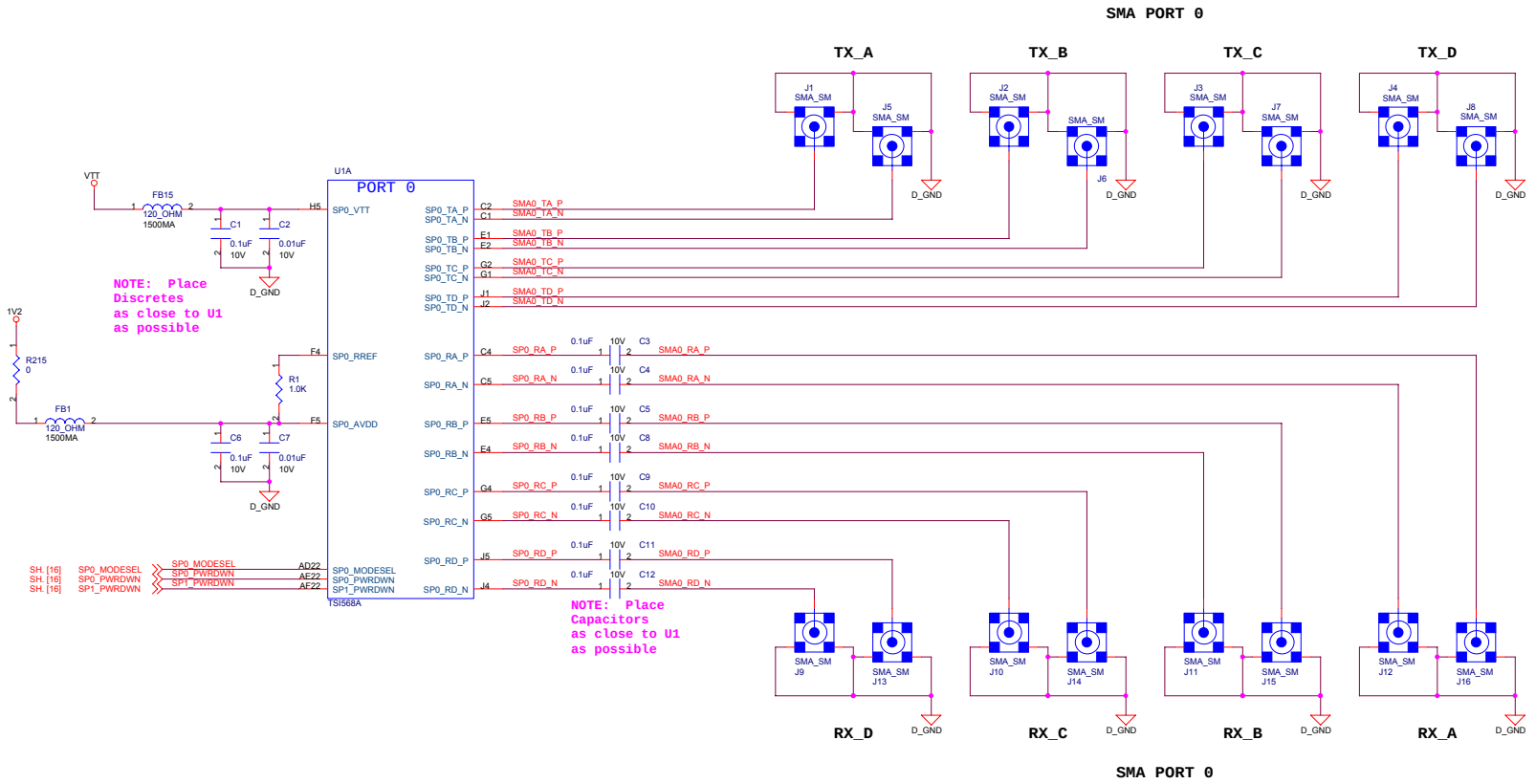

SMA Interface 0			
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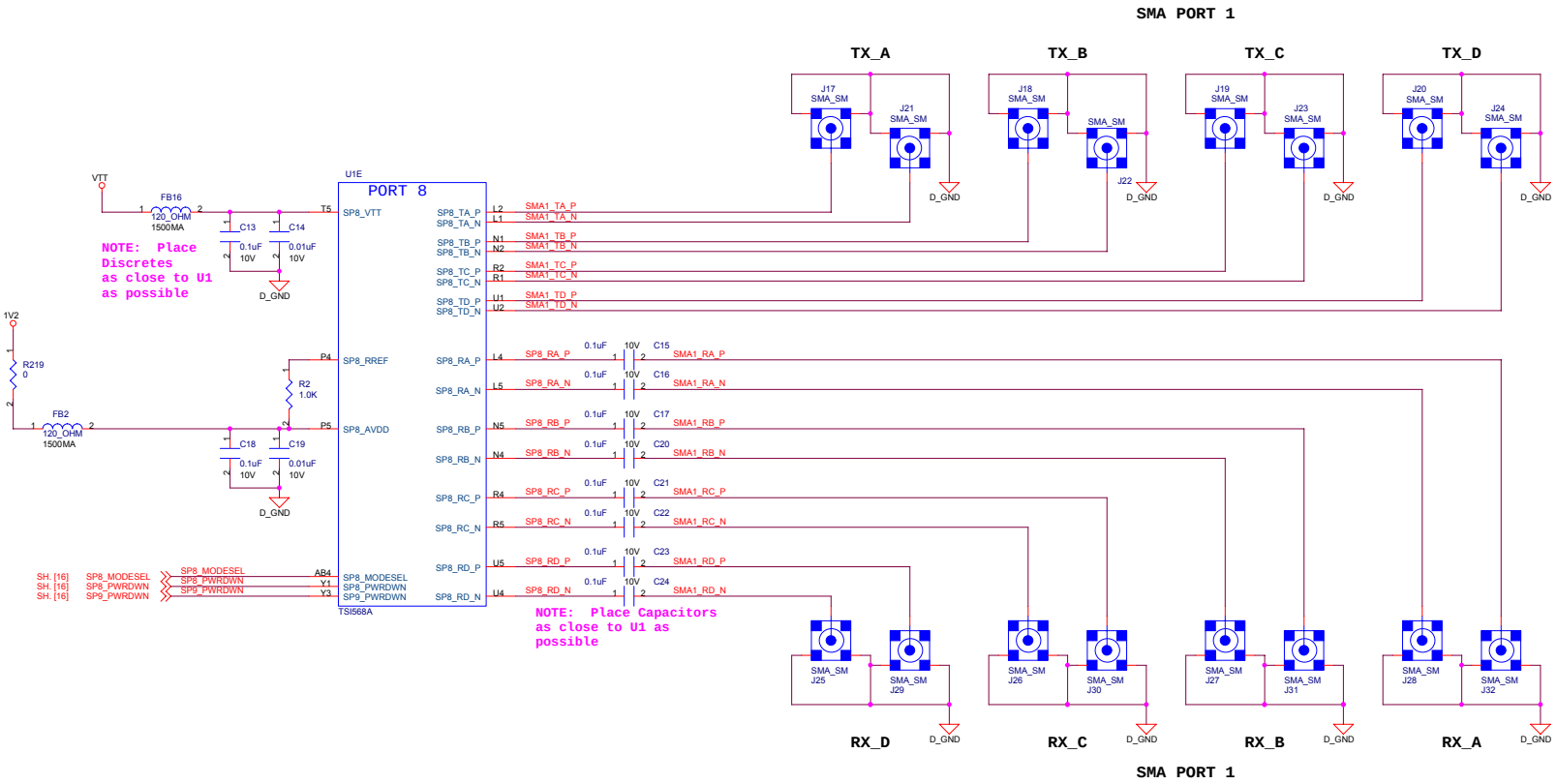

SMA Interface 1			
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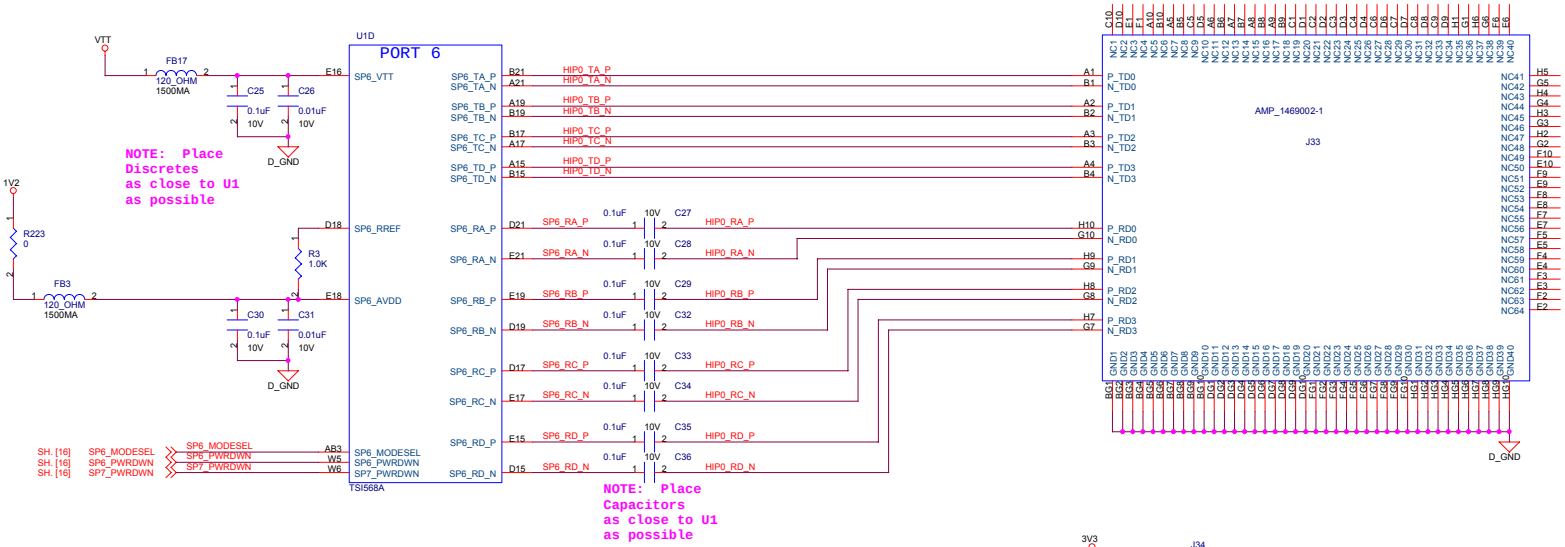
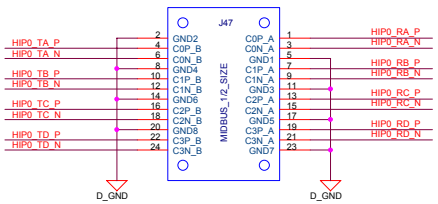
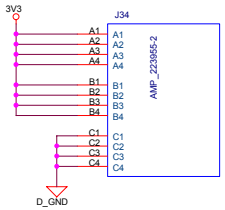
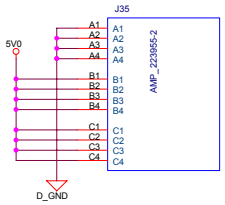
SRIO / HIP Connectors



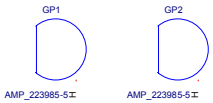
SRIO TEST CONNECTOR







SRIO / HIP Guide Pins



SRIO / HIP Interface		
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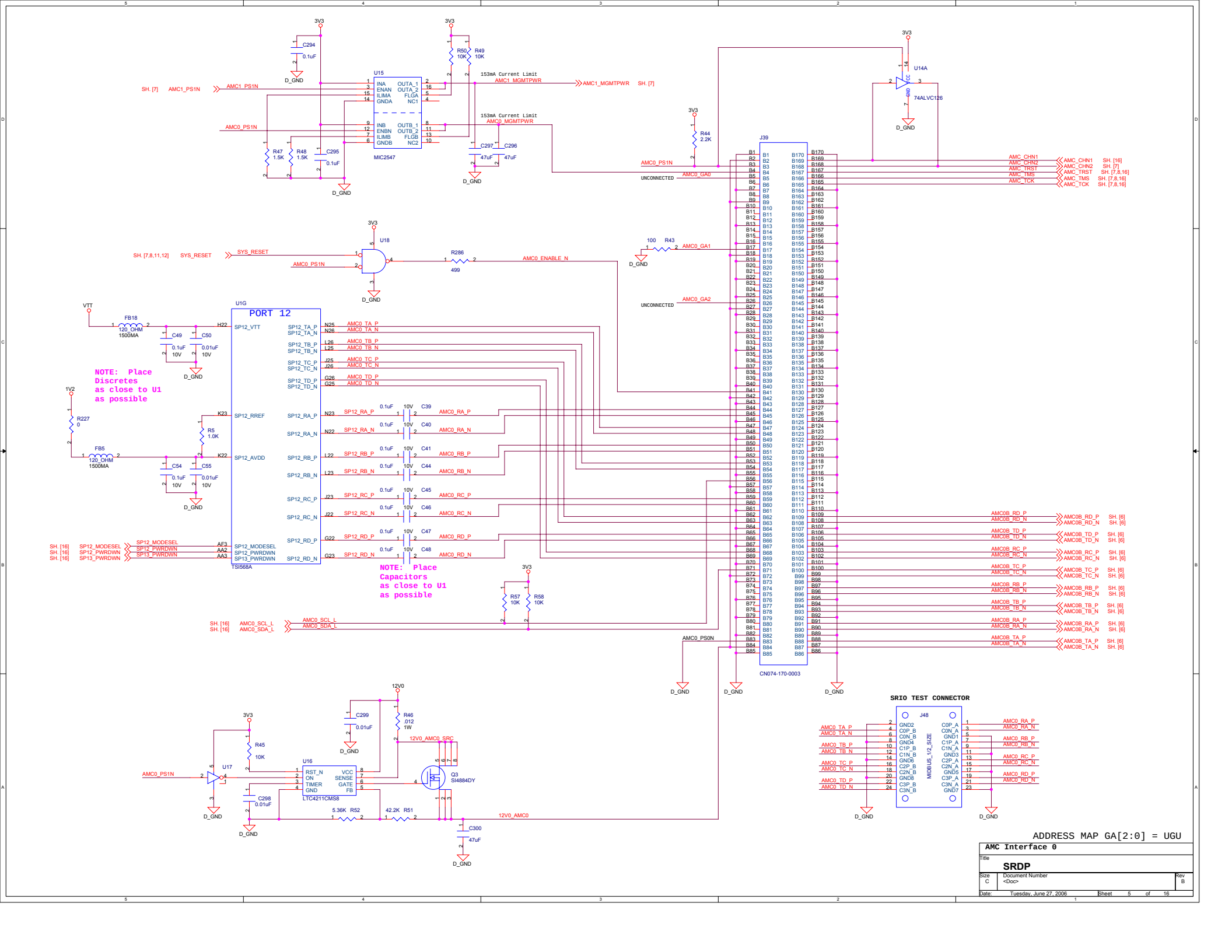
3V3
C294
0.1uF
D_GND
U15
INA
ENAN
ILIMA
GNDA
OUTA_1
OUTA_2
FLGA
NC1
INB
ENBN
ILIMB
GNDB
OUTB_1
OUTB_2
FLGB
NC2
MIC2547
R50
10K
R49
10K
153mA Current Limit
AMC1_MGMTPWR
SH. [7]
AMC1_PS1N
AMC0_PS1N
R47
1.5K
R48
1.5K
C295
0.1uF
153mA Current Limit
AMC0_MGMTPWR
C297
47uF
C296
47uF
R44
2.2K
U14A
74ALVC126
J39
AMC0_PS1N
UNCONNECTED
AMC0_GA0
AMC0_GA2
AMC_CHN1
AMC_CHN2
AMC_TRST
AMC_TMS
AMC_TCK
U18
SYS_RESET
SH. [7,8,11,12]
R286
499
AMC0_ENABLE_N
R43
100
U1G
PORT 12
TSI568A
VTT
FB18
120_OHM
1500MA
C49
C50
0.1uF
10V
0.01uF
10V
NOTE: Place
Discretes
as close to U1
as possible
1V2
R227
0
R5
1.0K
FB5
120_OHM
1500MA
C54
C55
SP12_VTT
SP12_RREF
SP12_AVDD
SP12_TA_P
SP12_TA_N
SP12_TB_P
SP12_TB_N
SP12_TC_P
SP12_TC_N
SP12_TD_P
SP12_TD_N
SP12_RA_P
SP12_RA_N
SP12_RB_P
SP12_RB_N
SP12_RC_P
SP12_RC_N
SP12_RD_P
SP12_RD_N
AMC0_TA_P
AMC0_TA_N
AMC0_TB_P
AMC0_TB_N
AMC0_TC_P
AMC0_TC_N
AMC0_TD_P
AMC0_TD_N
AMC0_RA_P
AMC0_RA_N
AMC0_RB_P
AMC0_RB_N
AMC0_RC_P
AMC0_RC_N
AMC0_RD_P
AMC0_RD_N
C39
C40
C41
C44
C45
C46
C47
C48
SP12_MODESEL
SP12_PWRDWN
SP13_PWRDWN
NOTE: Place
Capacitors
as close to U1
as possible
R57
10K
R58
10K
AMC0_SCL_L
AMC0_SDA_L
AMC0_PS0N
CN074-170-0003
AMC0B_RD_P
AMC0B_RD_N
AMC0B_TD_P
AMC0B_TD_N
AMC0B_RC_P
AMC0B_RC_N
AMC0B_TC_P
AMC0B_TC_N
AMC0B_RB_P
AMC0B_RB_N
AMC0B_TB_P
AMC0B_TB_N
AMC0B_RA_P
AMC0B_RA_N
AMC0B_TA_P
AMC0B_TA_N
SRIO TEST CONNECTOR
J48
MIDBUS_1/2_SIZE
12V0
U17
U16
LTC4211CMS8
RST_N
ON
TIMER
GND
VCC
SENSE
GATE
FB
R45
10K
C299
0.01uF
R46
.012
1W
12V0_AMC0_SRC
Q3
SI4884DY
C298
0.01uF
5.36K R52
42.2K R51
12V0_AMC0
C300
47uF
ADDRESS MAP GA[2:0] = UGU
AMC Interface 0
Title
SRDP
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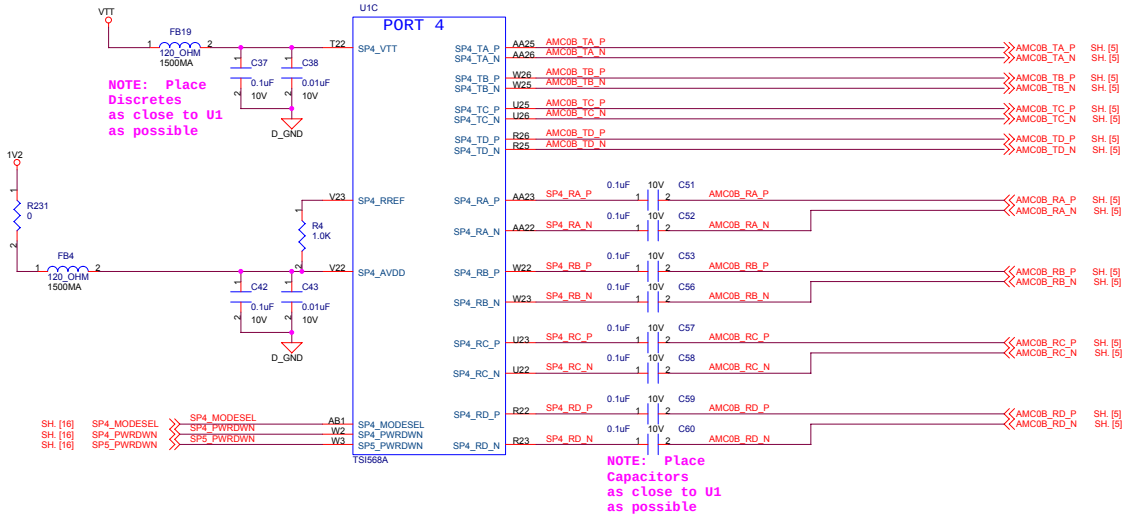

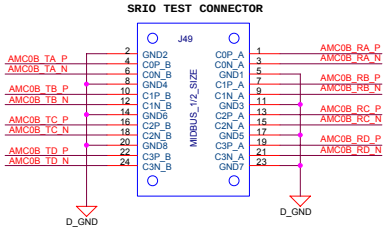

AMC Interface 0 continued

Title: SRDP

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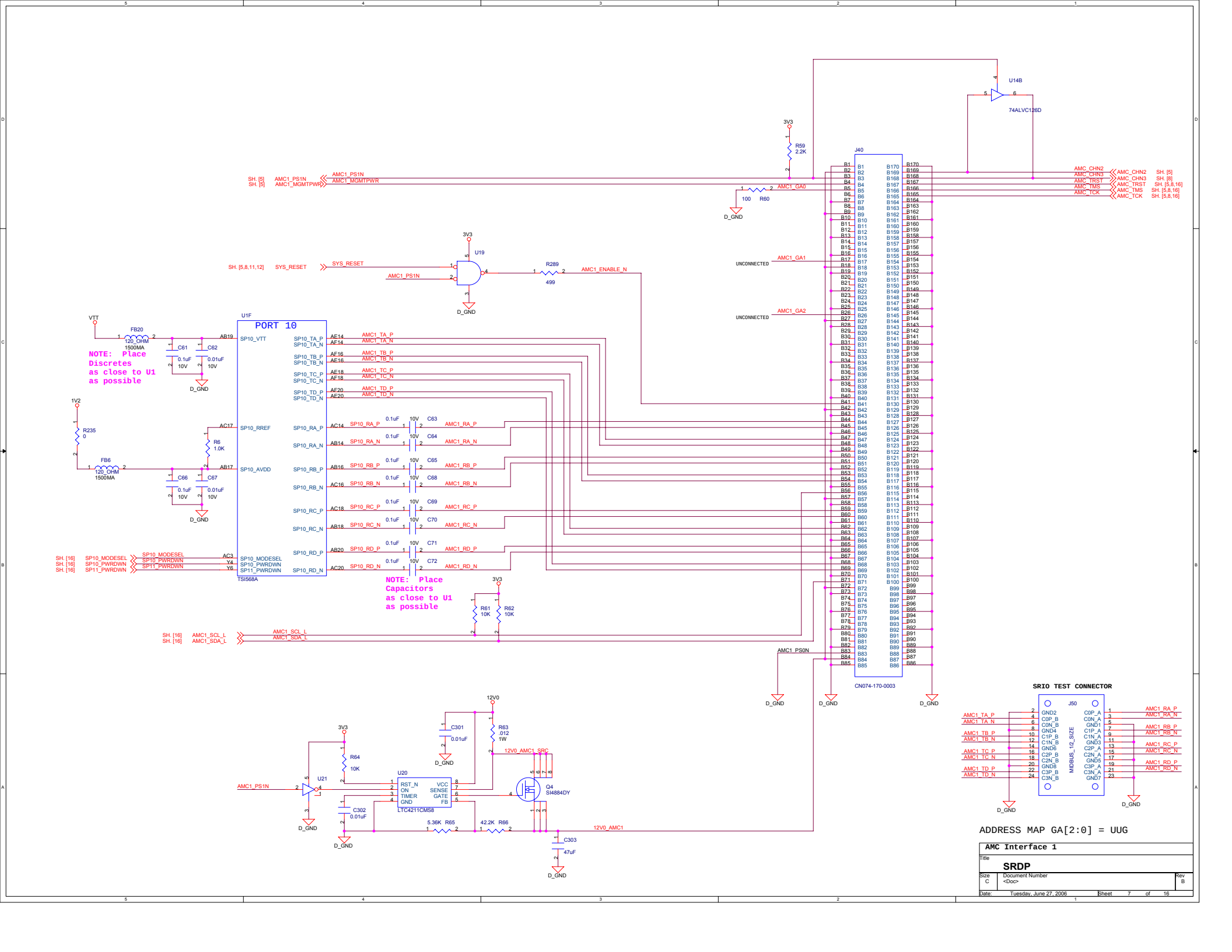
U14B
74ALVC126D
3V3
R59
2.2K
J40
CN074-170-0003
AMC1_PS1N
AMC1_MGMTPWR
AMC1_GA0
R60
100
D_GND
U19
SYS_RESET
R289
499
AMC1_ENABLE_N
AMC1_GA1
UNCONNECTED
AMC1_GA2
UNCONNECTED
AMC_CHN2
AMC_CHN3
AMC_TRST
AMC_TMS
AMC_TCK
U1F
PORT 10
TSI568A
VTT
FB20
120_OHM
1500MA
C61
C62
0.1uF
0.01uF
10V
NOTE: Place Discretes as close to U1 as possible
1V2
R235
0
R6
1.0K
FB6
C66
C67
SP10_MODESEL
SP10_PWRDWN
SP11_PWRDWN
NOTE: Place Capacitors as close to U1 as possible
R61
10K
R62
10K
AMC1_SCL_L
AMC1_SDA_L
AMC1_PS0N
SRIO TEST CONNECTOR
J50
MIDBUS_1/2_SIZE
U21
U20
LTC4211CMS8
RST_N
ON
TIMER
GND
VCC
SENSE
GATE
FB
Q4
SI4884DY
12V0
12V0_AMC1_SRC
12V0_AMC1
C301
0.01uF
R63
.012
1W
R64
10K
C302
0.01uF
5.36K
R65
42.2K
R66
C303
47uF
ADDRESS MAP GA[2:0] = UUG
AMC Interface 1
SRDP
Size C
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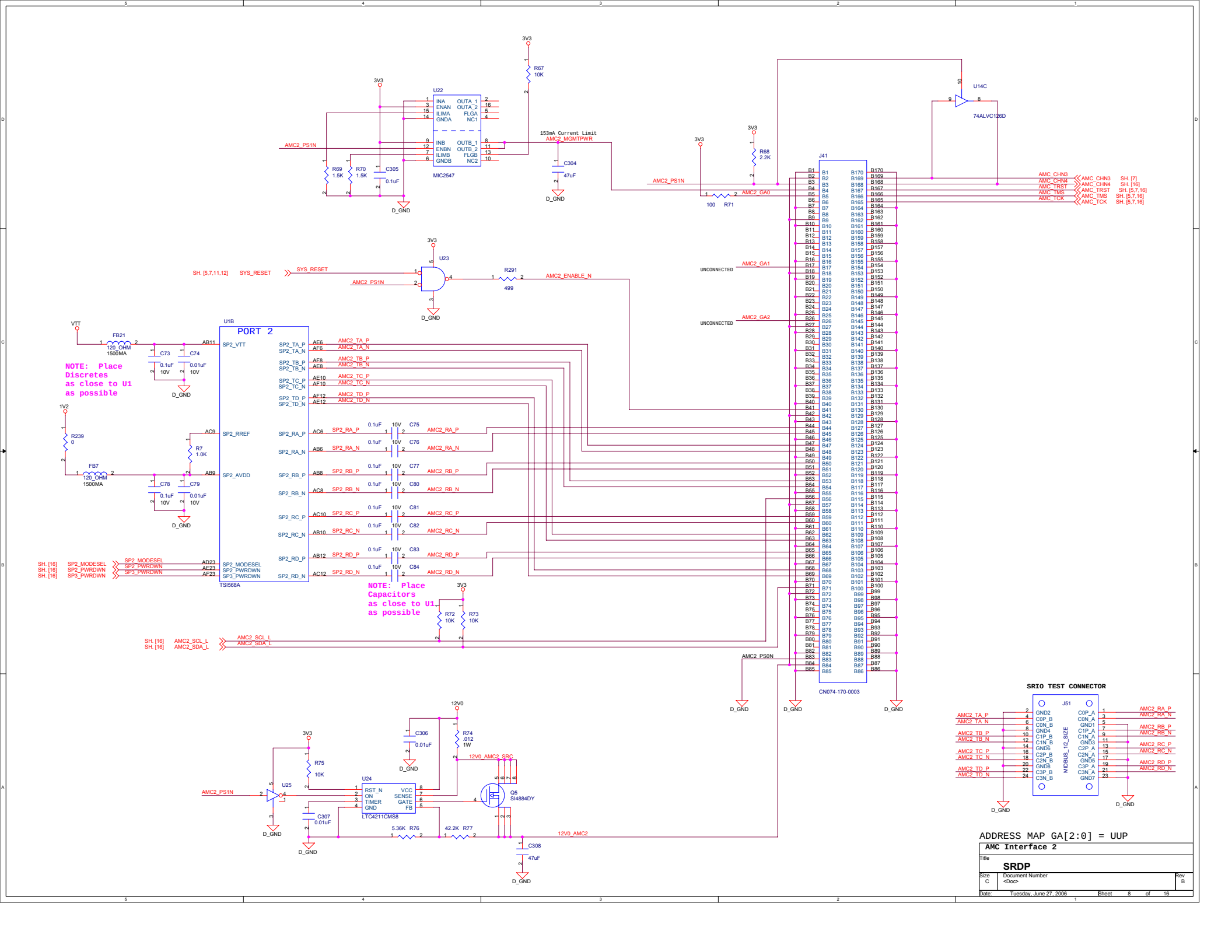
U22
MIC2547
AMC2_PS1N
153mA Current Limit
AMC2_MGMTPWR
R67 10K
R68 2.2K
R69 1.5K
R70 1.5K
C305 0.1uF
C304 47uF
U14C
74ALVC126D
J41
CN074-170-0003
AMC2_GA0
AMC2_GA1
AMC2_GA2
UNCONNECTED
100 R71
U23
SYS_RESET
AMC2_ENABLE_N
R291 499
U1B
PORT 2
TSI568A
NOTE: Place Discretes as close to U1 as possible
NOTE: Place Capacitors as close to U1 as possible
FB21 120_OHM 1500MA
FB7 120_OHM 1500MA
R239 0
R7 1.0K
R72 10K
R73 10K
AMC2_SCL_L
AMC2_SDA_L
AMC2_PS0N
U25
U24
LTC4211CMS8
Q5 SI4884DY
R74 .012 1W
R75 10K
C306 0.01uF
C307 0.01uF
R76 5.36K
R77 42.2K
C308 47uF
12V0_AMC2_SRC
12V0_AMC2
SRIO TEST CONNECTOR
J51
MDBUS_1/2_SIZE
ADDRESS MAP GA[2:0] = UUP
AMC Interface 2
SRDP
Size C
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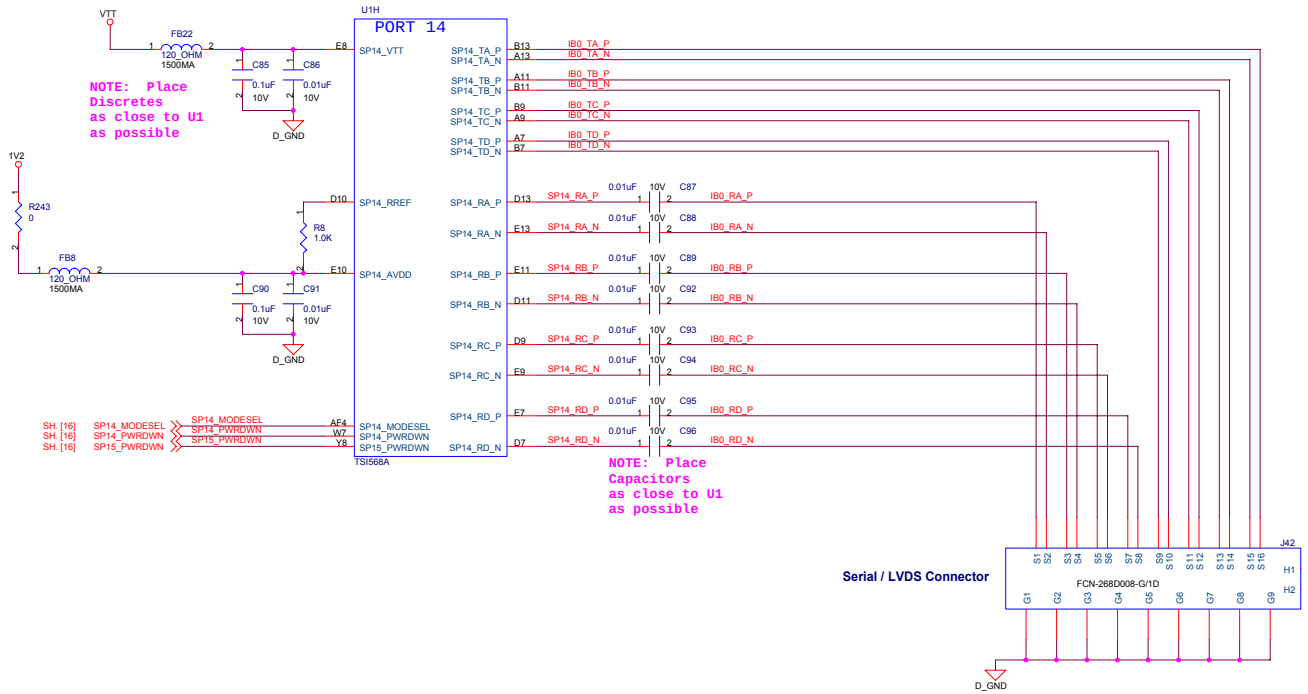

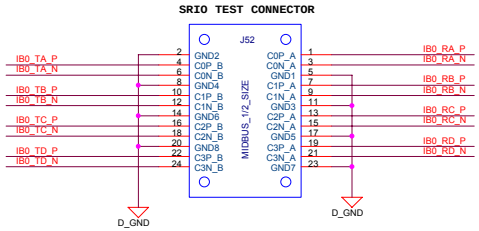

4x I/O Differential Cable Connector			
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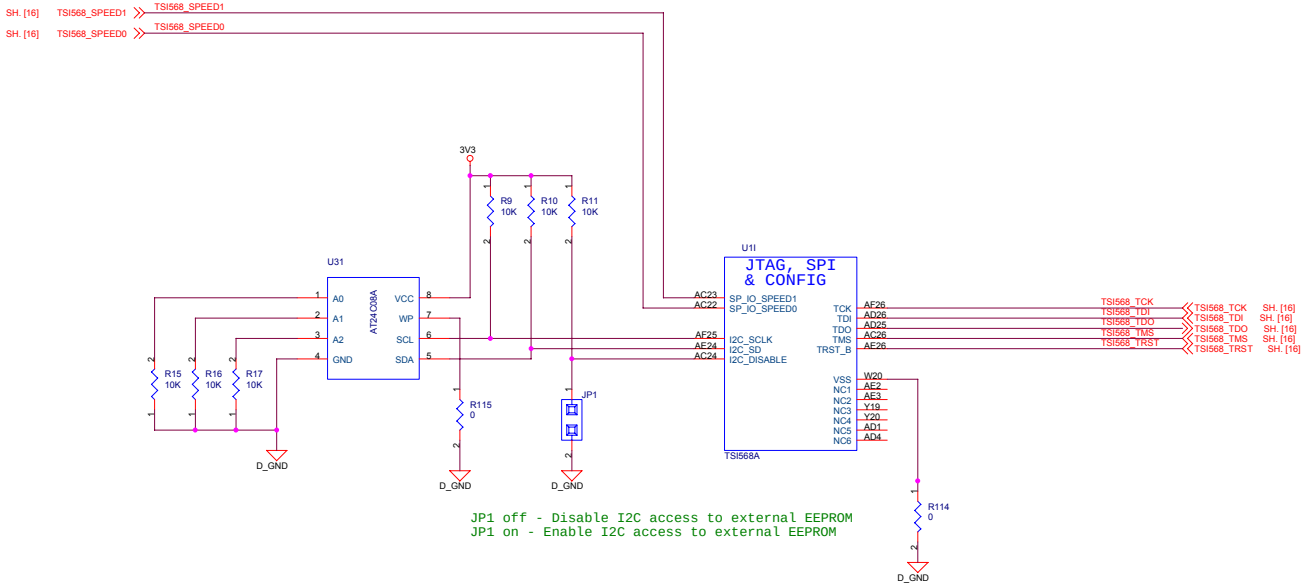

JTAG & Configuration			
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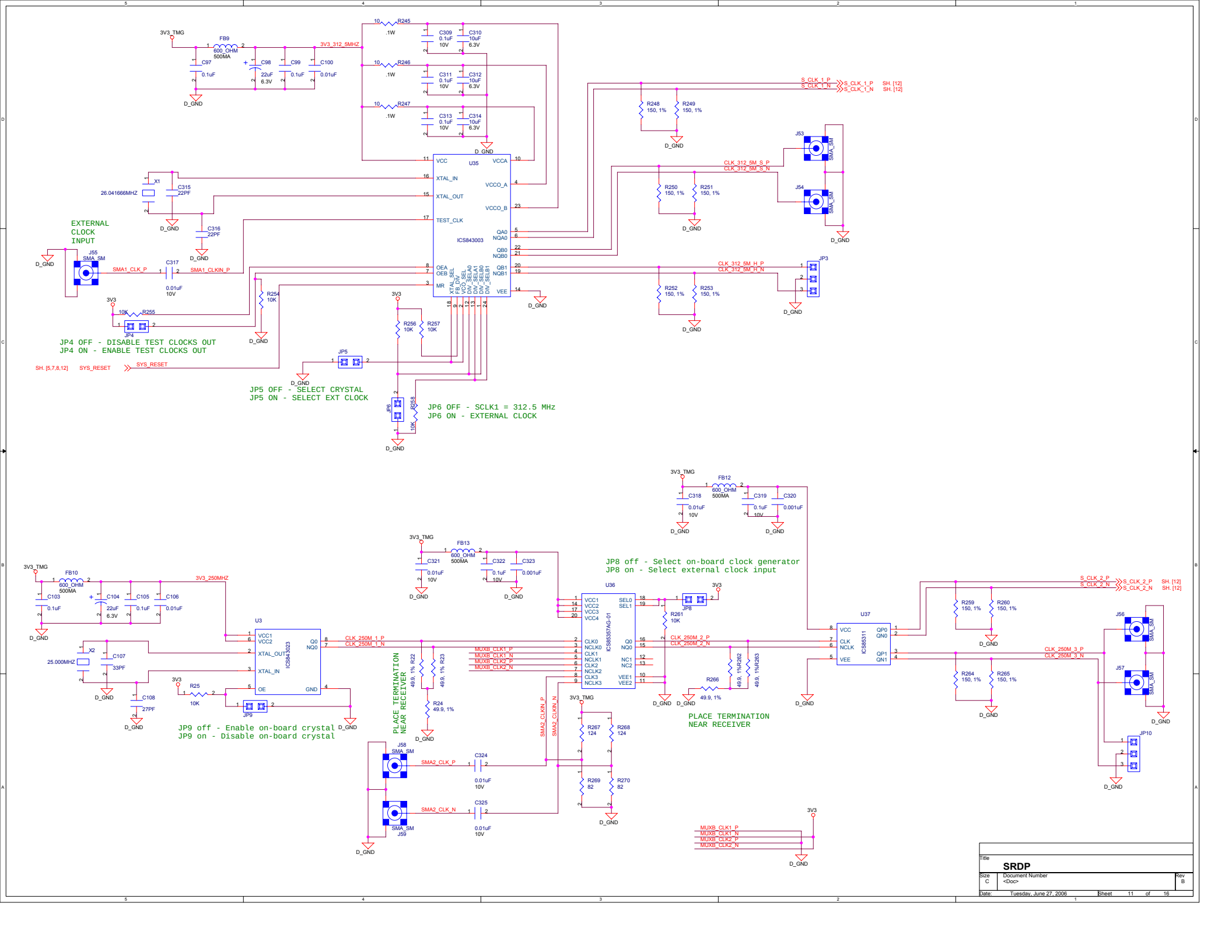
3V3_TMG
FB9
600_OHM
500MA
3V3_312_5MHZ
C97
0.1uF
C98
22uF
6.3V
C99
0.1uF
C100
0.01uF
D_GND
R245
.1W
R246
R247
C309
0.1uF
10V
C310
10uF
6.3V
C311
C312
C313
C314
U35
ICS843003
VCC
VCCA
XTAL_IN
XTAL_OUT
VCCO_A
VCCO_B
TEST_CLK
QA0
NQA0
QB0
NQB0
OEA
OEB
MR
QB1
NQB1
VEE
X1
26.041666MHZ
C315
22PF
C316
EXTERNAL
CLOCK
INPUT
J55
SMA_SM
SMA1_CLK_P
SMA1_CLKIN_P
C317
0.01uF
R254
10K
R255
JP4
JP4 OFF - DISABLE TEST CLOCKS OUT
JP4 ON - ENABLE TEST CLOCKS OUT
SH. [5,7,8,12]
SYS_RESET
JP5
JP5 OFF - SELECT CRYSTAL
JP5 ON - SELECT EXT CLOCK
R256
R257
JP6
R258
JP6 OFF - SCLK1 = 312.5 MHz
JP6 ON - EXTERNAL CLOCK
S_CLK_1_P
S_CLK_1_N
SH. [12]
R248
150, 1%
R249
J53
J54
SMA_SM
CLK_312_5M_S_P
CLK_312_5M_S_N
R250
R251
CLK_312_5M_H_P
CLK_312_5M_H_N
JP3
R252
R253
FB10
3V3_250MHZ
C103
C104
C105
C106
U3
ICS843023
VCC1
VCC2
XTAL_OUT
XTAL_IN
OE
GND
Q0
NQ0
X2
25.000MHZ
C107
33PF
C108
27PF
R25
JP9
JP9 off - Enable on-board crystal
JP9 on - Disable on-board crystal
FB13
C321
C322
C323
FB12
C318
C319
C320
JP8 off - Select on-board clock generator
JP8 on - Select external clock input
U36
IC585357AG-01
SEL0
SEL1
CLK0
NCLK0
CLK1
NCLK1
CLK2
NCLK2
CLK3
NCLK3
NC1
NC2
VEE1
VEE2
JP8
R261
CLK_250M_1_P
CLK_250M_1_N
CLK_250M_2_P
CLK_250M_2_N
MUXB_CLK1_P
MUXB_CLK1_N
MUXB_CLK2_P
MUXB_CLK2_N
R24
R23
R22
R262
R263
R266
PLACE TERMINATION
NEAR RECEIVER
U37
IC585311
QP0
QN0
QP1
QN1
R259
R260
R264
R265
J56
J57
CLK_250M_3_P
CLK_250M_3_N
JP10
J58
J59
SMA2_CLK_P
SMA2_CLK_N
C324
C325
R267
R268
R269
R270
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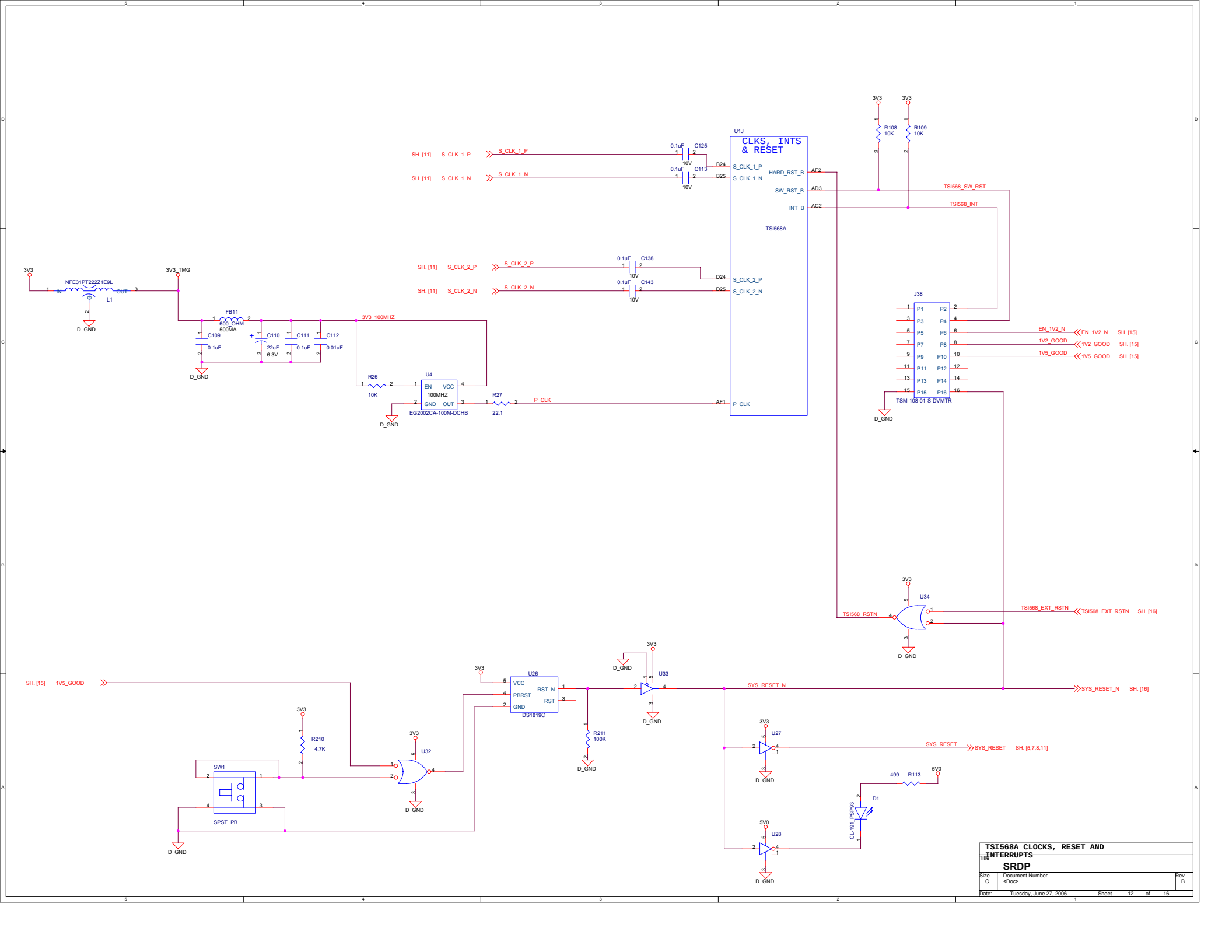
U1J
CLKS, INTS & RESET
TSI568A
S_CLK_1_P
S_CLK_1_N
S_CLK_2_P
S_CLK_2_N
HARD_RST_B
SW_RST_B
INT_B
P_CLK
TSI568_SW_RST
TSI568_INT
R108 10K
R109 10K
C125 0.1uF
C113 0.1uF
C138 0.1uF
C143 0.1uF
NFE31PT222Z1E9L
L1
FB11 600_OHM 500MA
C109 0.1uF
C110 22uF 6.3V
C111 0.1uF
C112 0.01uF
3V3_100MHZ
U4
EG2002CA-100M-DCHB
100MHZ
R26 10K
R27 22.1
J38
TSM-108-01-S-DVMTR
EN_1V2_N
1V2_GOOD
1V5_GOOD
U34
TSI568_RSTN
TSI568_EXT_RSTN
U26
DS1819C
U33
SYS_RESET_N
U27
SYS_RESET
U28
U32
R210 4.7K
R211 100K
SW1
SPST_PB
R113 499
D1
CL-191_RSP33
TSI568A CLOCKS, RESET AND INTERRUPTS
SRDP
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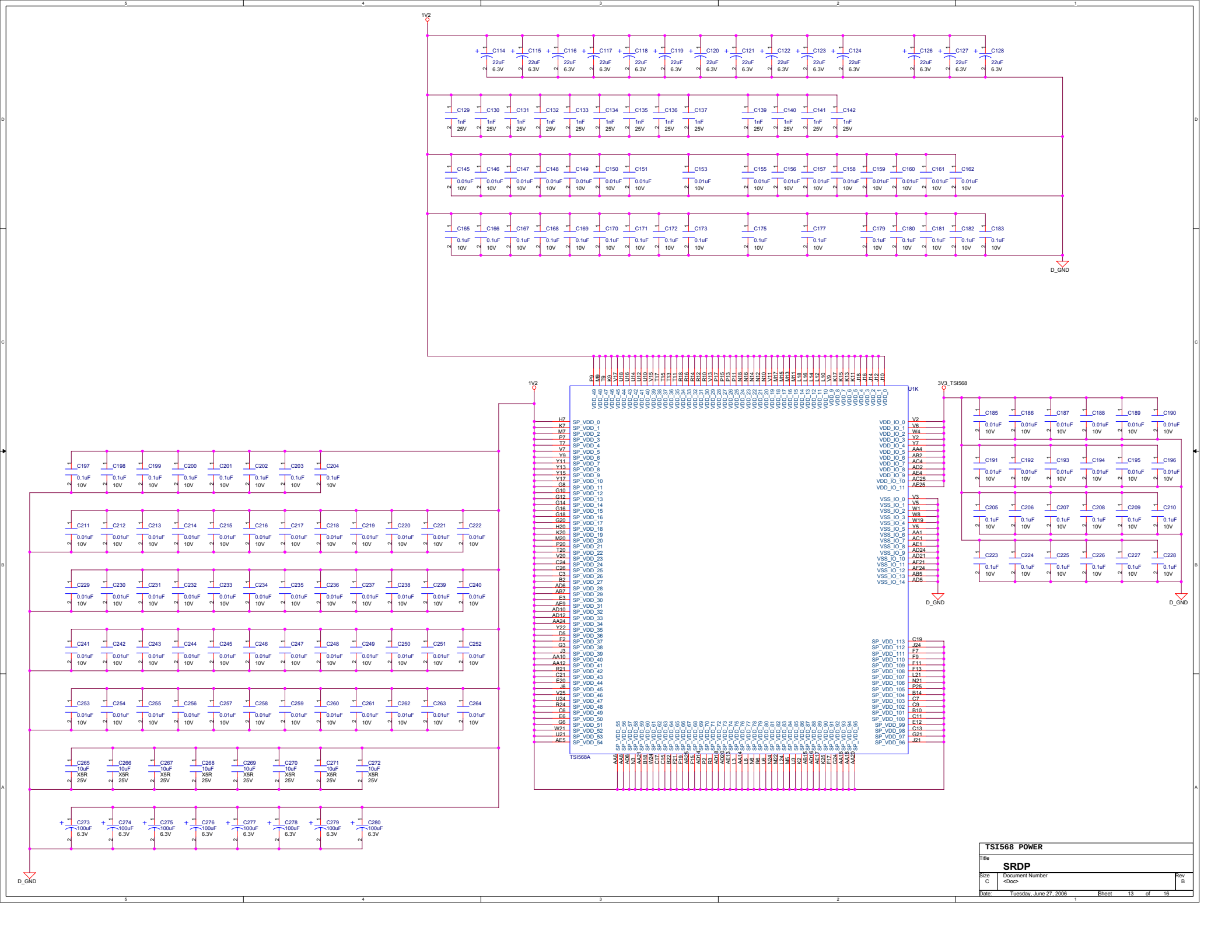

TSI568 POWER			
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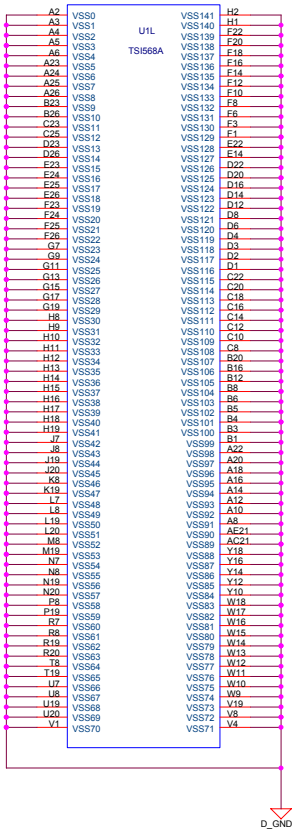

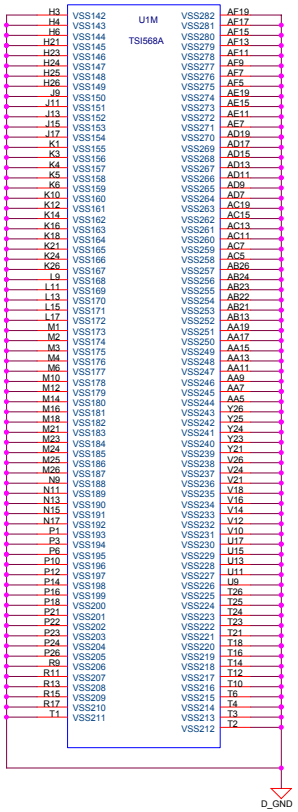

TSI568 GROUNDS

Title

SRDP

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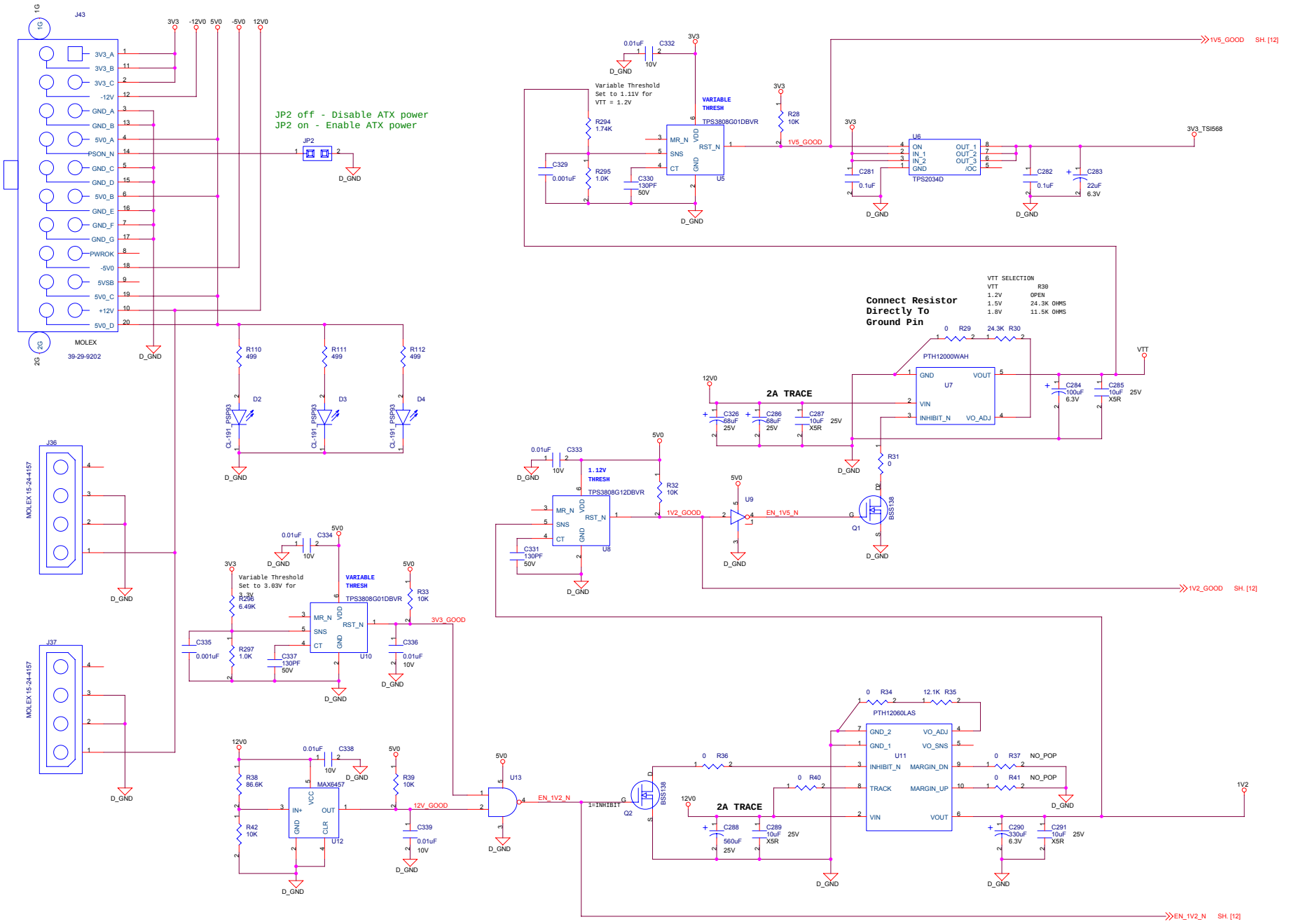
J43
MOLEX
39-29-9202
JP2 off - Disable ATX power
JP2 on - Enable ATX power
JP2
D_GND
R110 499
R111 499
R112 499
D2
D3
D4
CL-191 PSP93
J36
J37
MOLEX 15-24-4157
Variable Threshold
Set to 1.11V for
VTT = 1.2V
Variable Threshold
Set to 3.03V for
3.3V
VARIABLE THRESH
TPS3808G01DBVR
TPS3808G12DBVR
R294 1.74K
R295 1.0K
R28 10K
R32 10K
R33 10K
R296 6.49K
R297 1.0K
R38 86.6K
R42 10K
R39 10K
C329 0.001uF
C330 130PF 50V
C331 130PF 50V
C332 0.01uF 10V
C333 0.01uF 10V
C334 0.01uF 10V
C335 0.001uF
C336 0.01uF 10V
C337 130PF 50V
C338 0.01uF 10V
C339 0.01uF 10V
U5
U8
U10
U12
MAX6457
1V5_GOOD
1V2_GOOD
3V3_GOOD
12V_GOOD
EN_1V5_N
EN_1V2_N
1=INHIBIT
U6
TPS2034D
C281 0.1uF
C282 0.1uF
C283 22uF 6.3V
3V3_TSI568
VTT SELECTION
VTT R30
1.2V OPEN
1.5V 24.3K OHMS
1.8V 11.5K OHMS
Connect Resistor
Directly To
Ground Pin
PTH12000WAH
U7
R29 24.3K
R30
R31 0
C284 100uF 6.3V
C285 10uF X5R 25V
C286 68uF 25V
C287 10uF X5R 25V
C326 68uF 25V
2A TRACE
U9
Q1
BSS138
PTH12060LAS
U11
R34 12.1K
R35
R36
R37 NO_POP
R40
R41 NO_POP
C288 560uF 25V
C289 10uF X5R 25V
C290 330uF 6.3V
C291 10uF X5R 25V
Q2
U13
1V2
1V5_GOOD SH. [12]
1V2_GOOD SH. [12]
EN_1V2_N SH. [12]
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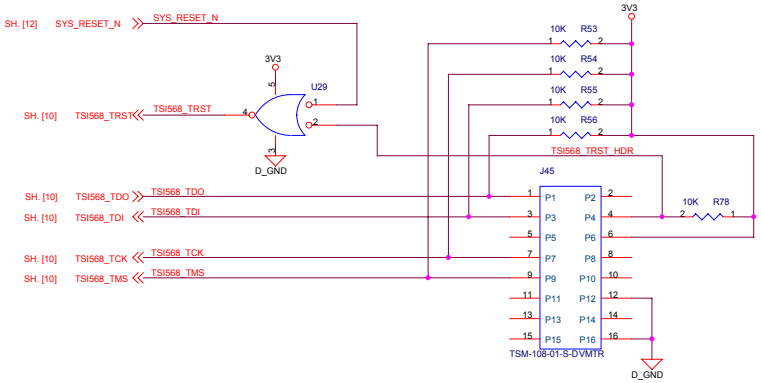
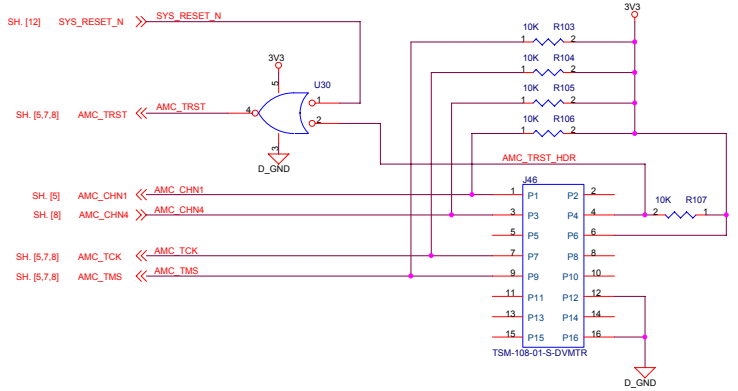
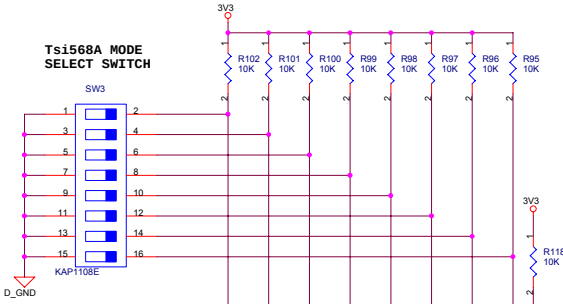
TSi568A JTAG INTERFACE

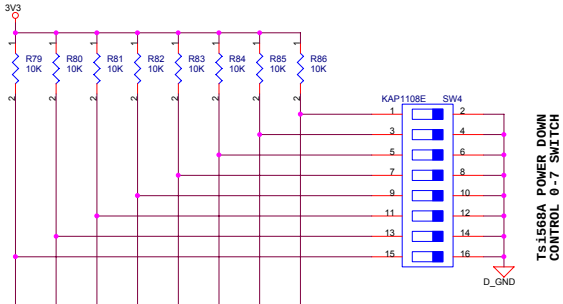


AMC JTAG INTERFACE

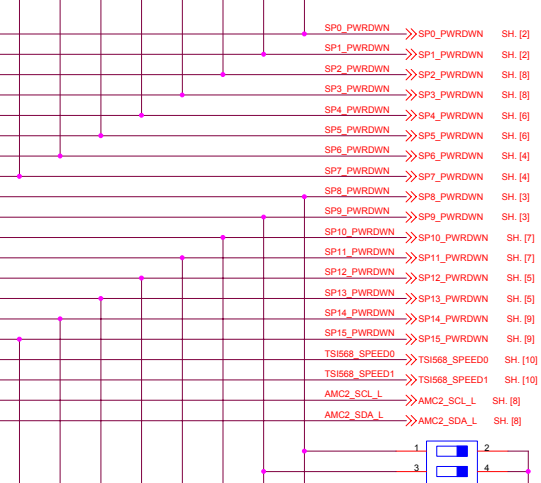


Tsi568A MODE SELECT SWITCH

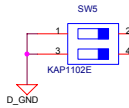




Tsi568A POWER DOWN CONTROL 0-7 SWITCH



Tsi568A SPEED CONTROL SWITCH



Tsi568A POWER DOWN CONTROL 8-15 SWITCH

CONTROL PROCESSOR INTERFACE

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