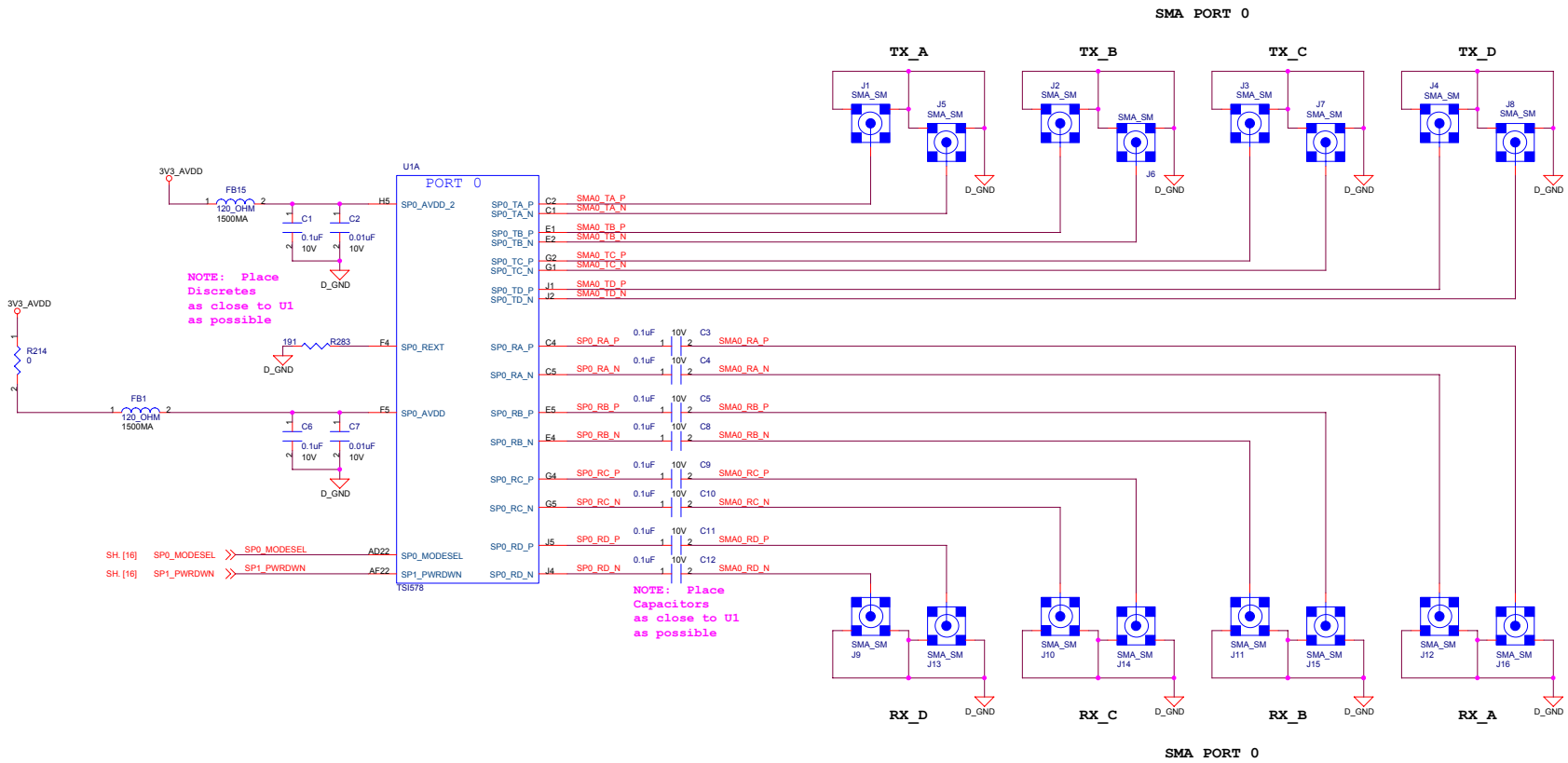


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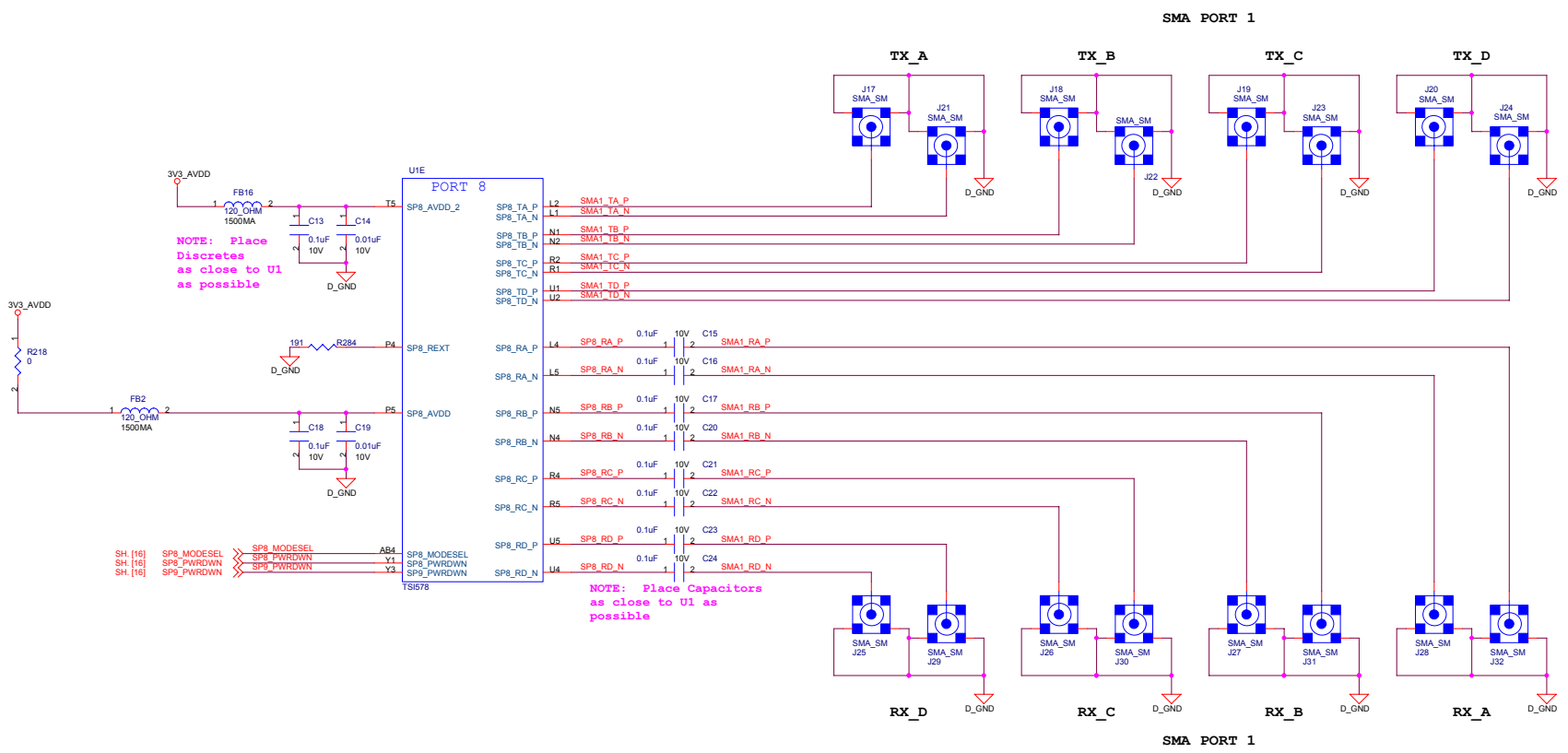
SHEET	TITLE	PAGE
SHEET 1	TITLE PAGE	
SHEET 2	SRIO SMA INTERFACE 0, TSi578 Port 0	
SHEET 3	SRIO SMA INTERFACE 1, TSi578 Port 8	
SHEET 4	SRIO HIP INTERFACE 0, TSi578 Port 6	
SHEET 5	SRIO AMC INTERFACE 0, TSi578 Port 12	
SHEET 6	SRIO AMC INTERFACE 0, TSi578 Port 4	
SHEET 7	SRIO AMC INTERFACE 1, TSi578 Port 10	
SHEET 8	SRIO AMC INTERFACE 2, TSi578 Port 2	
SHEET 9	Serial / LVDS Connector (4x), TSi578 Port 14	
SHEET 10	TSi578 JTAG AND CONFIGURATION PORTS	
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	- TSi578 JTAG INTERFACE	
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	- EXTERNAL CONTROL INTERFACE	
	- AMC JTAG INTERFACE	

Note A

This schematic is provided as a reference to be used in conjunction with the Serial RapidIO Development Platform (SRDP) board. This schematic is NOT to be used as reference design for IDT TSi57x platforms. Please refer to the appropriate device Hardware Manual for the specific requirements required for new designs.

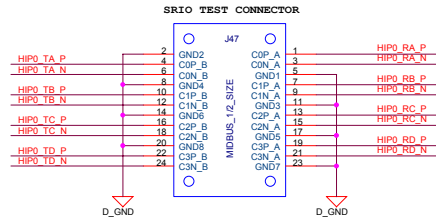
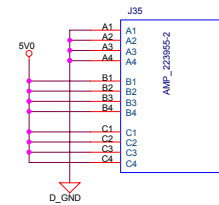
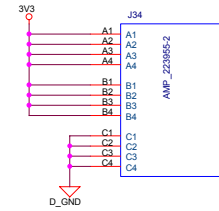
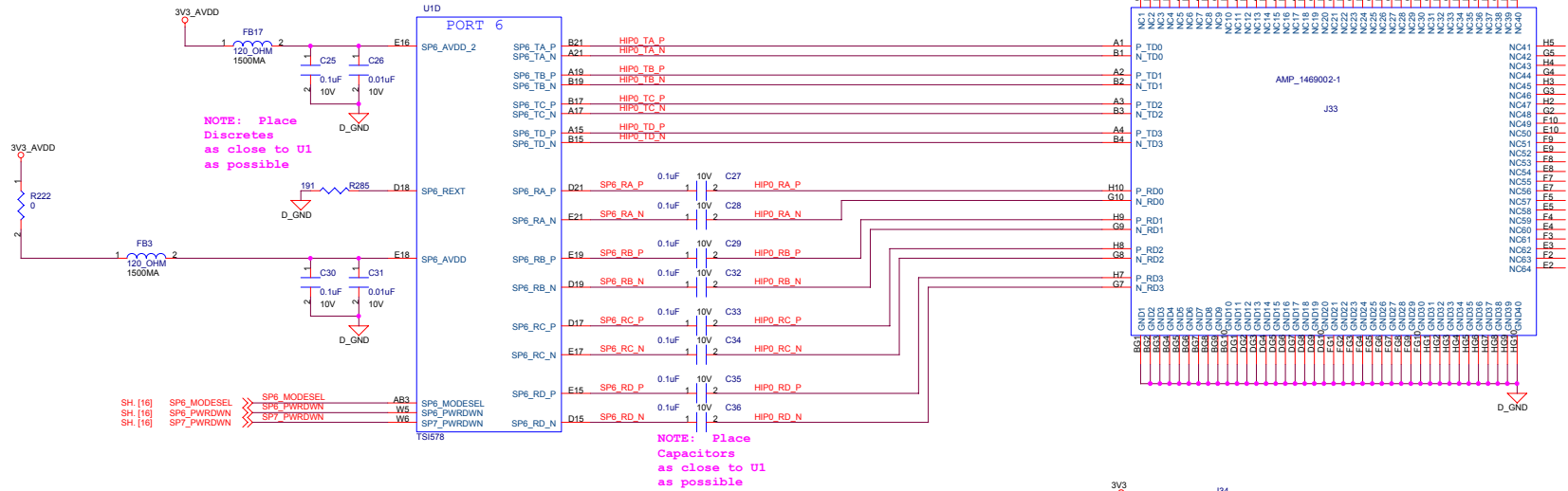


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SMA Interface 1			
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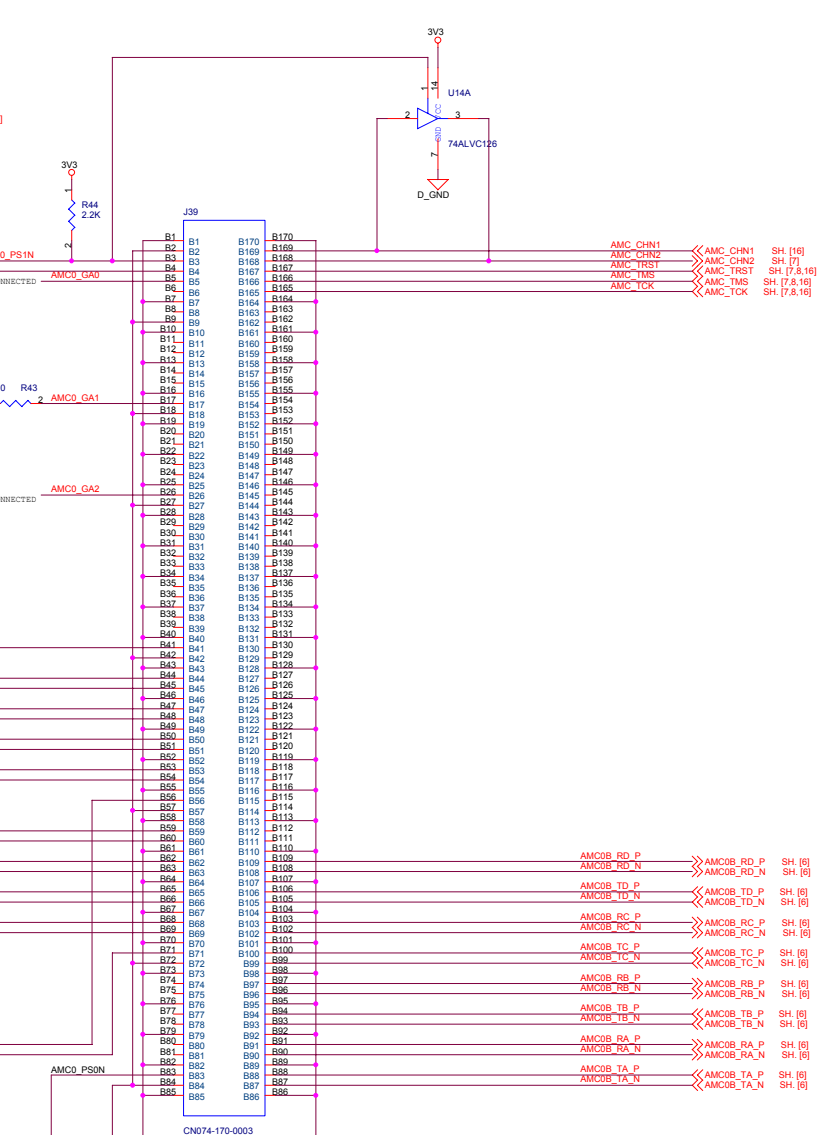
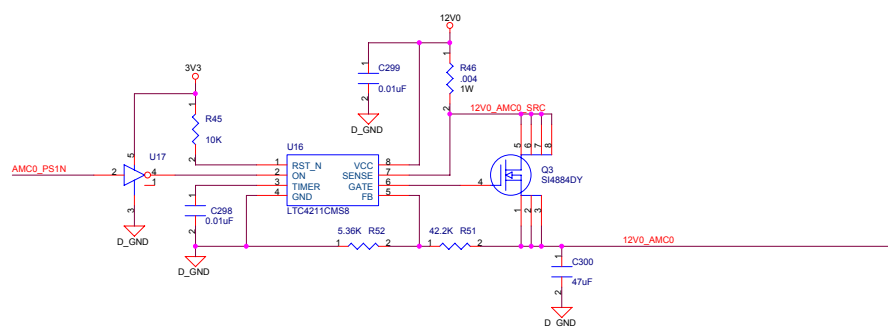
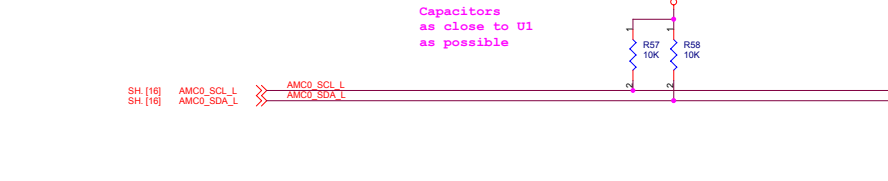
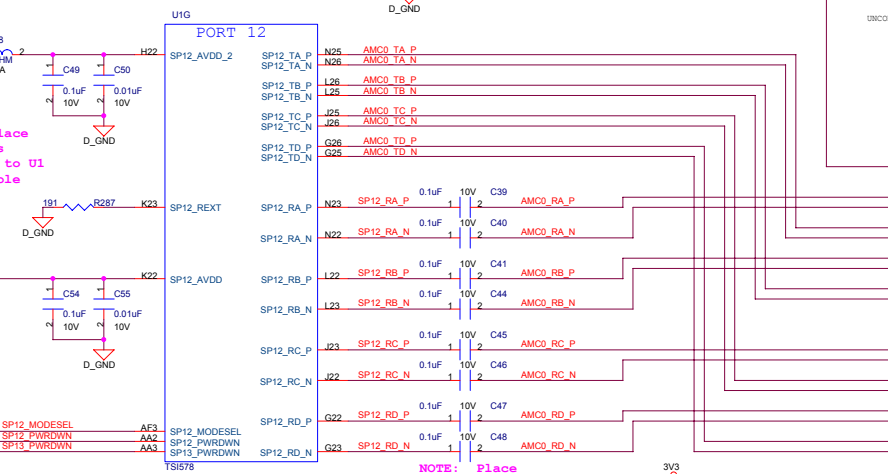
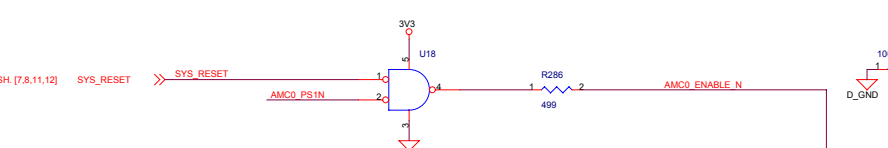
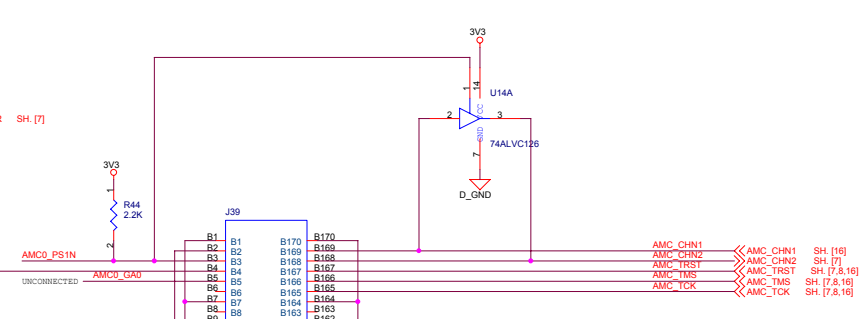
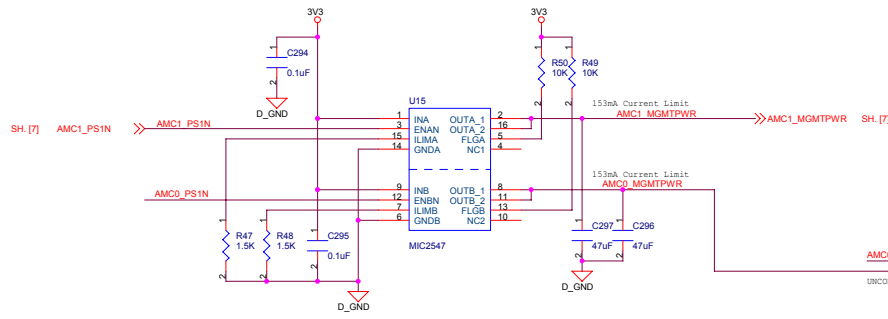
SRIO / HIP Connectors



SRIO / HIP Guide Pins

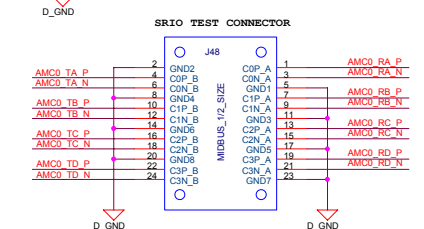


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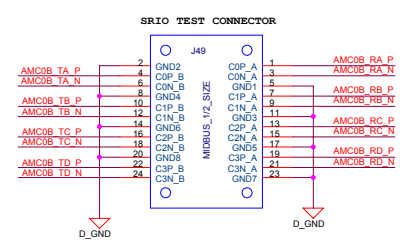
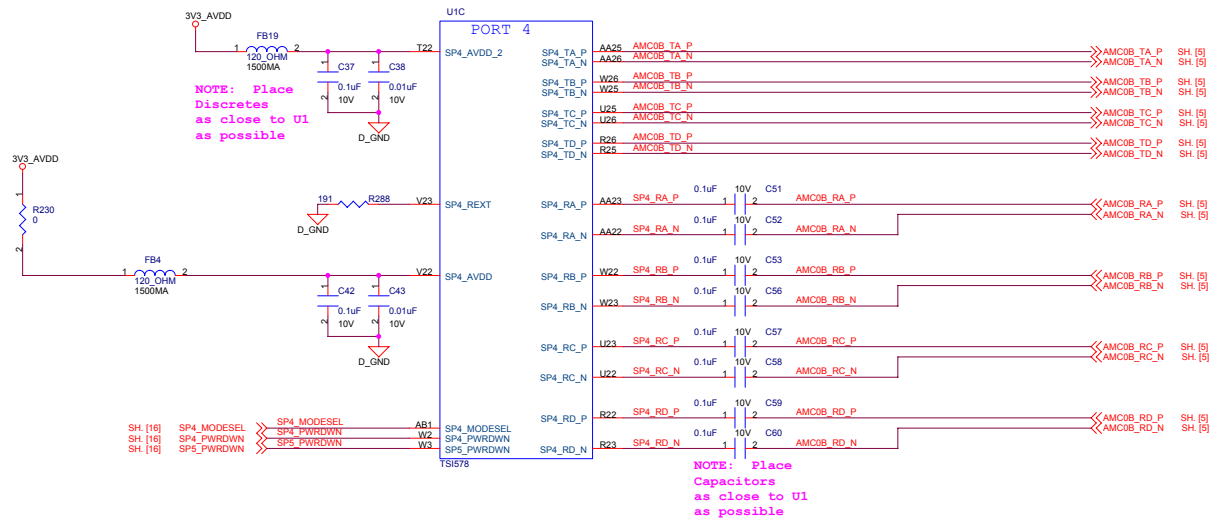
NOTE: Place Discretes as close to U1 as possible

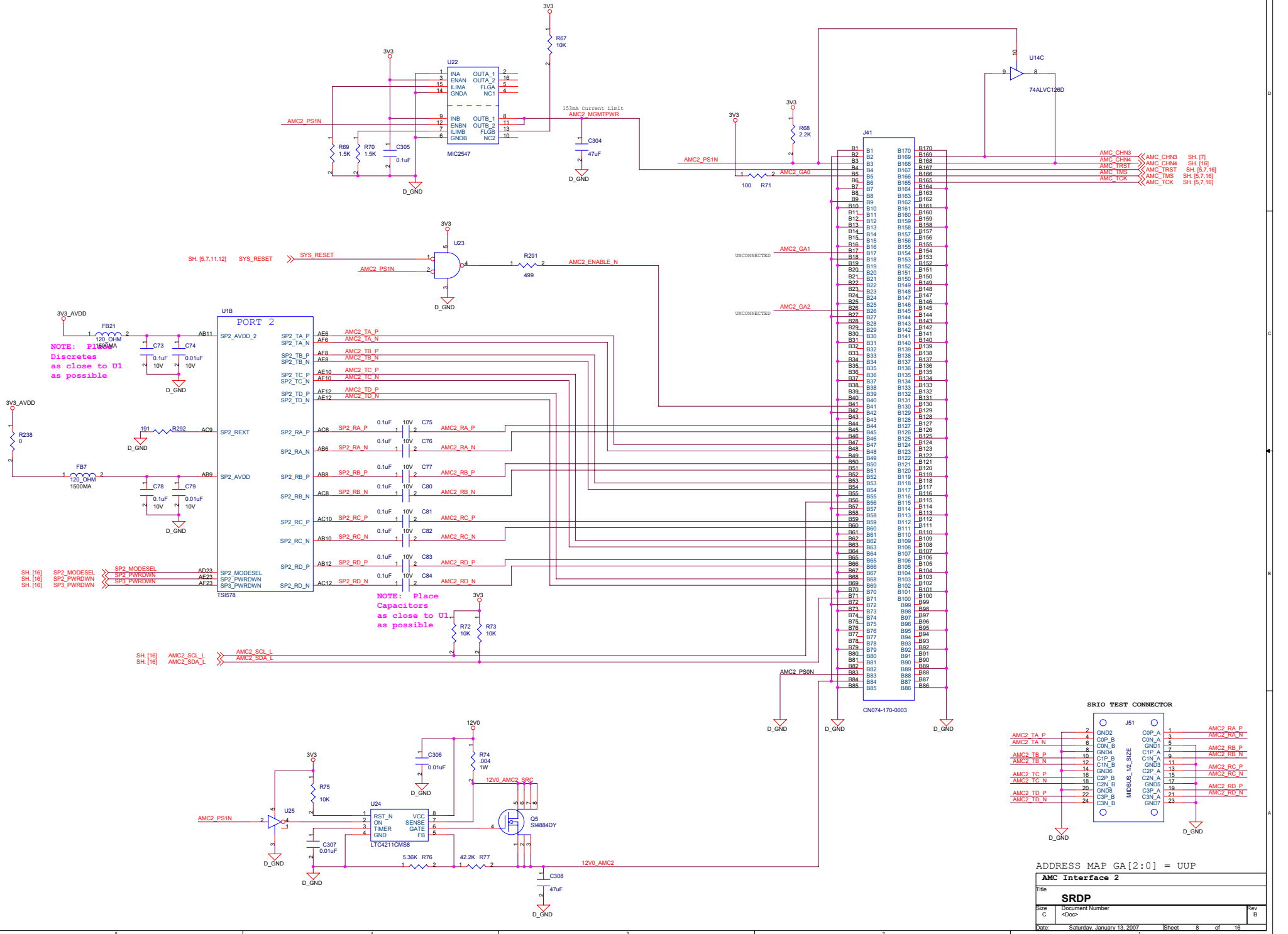
NOTE: Place Capacitors as close to U1 as possible



ADDRESS MAP GA[2:0] = UGU

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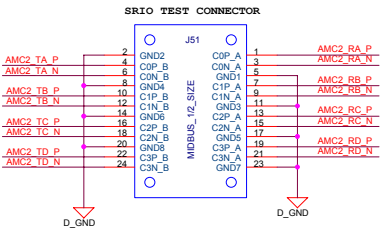




AMC2_CHN3 << AMC2_CHN3 SH [7]
 AMC2_CHN4 << AMC2_CHN4 SH [16]
 AMC2_TRST << AMC2_TRST SH [5,7,16]
 AMC2_TMS << AMC2_TMS SH [5,7,16]
 AMC2_TCK << AMC2_TCK SH [5,7,16]

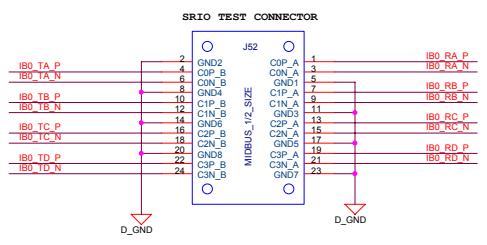
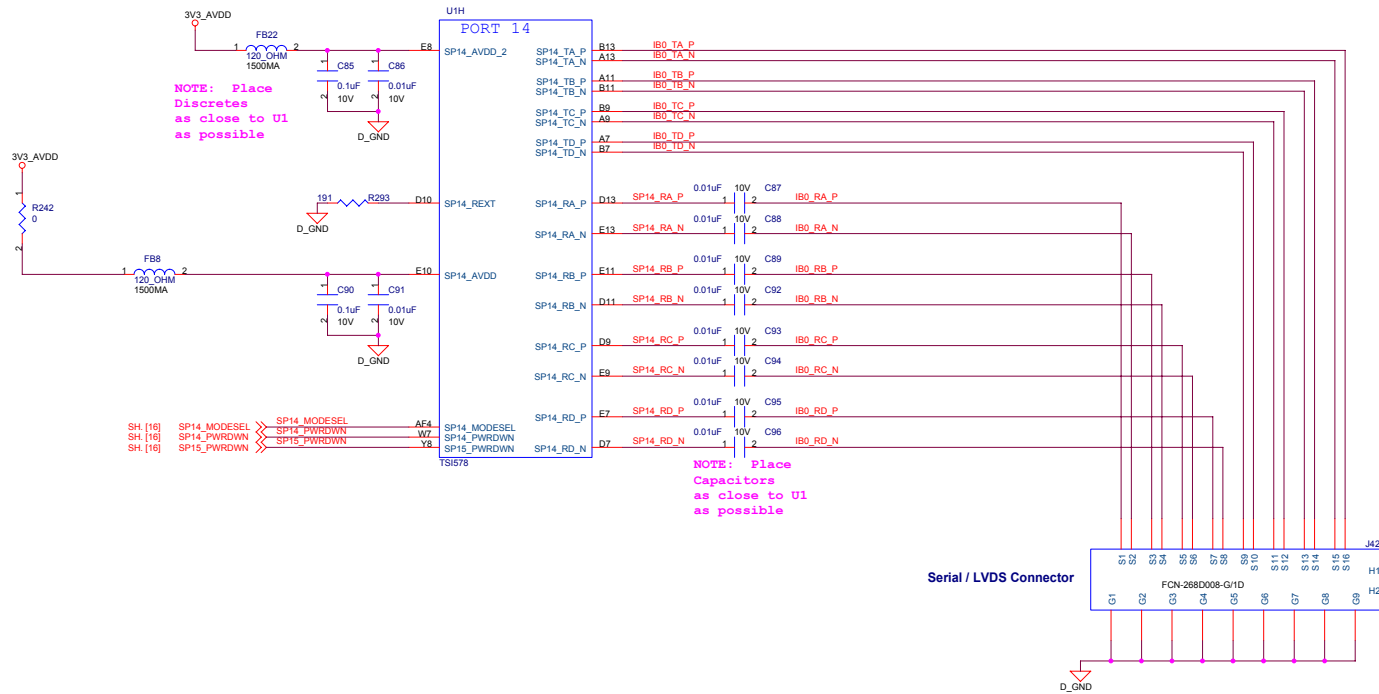
NOTE: Place
 Discretes
 as close to U1
 as possible

NOTE: Place
 Capacitors
 as close to U1
 as possible



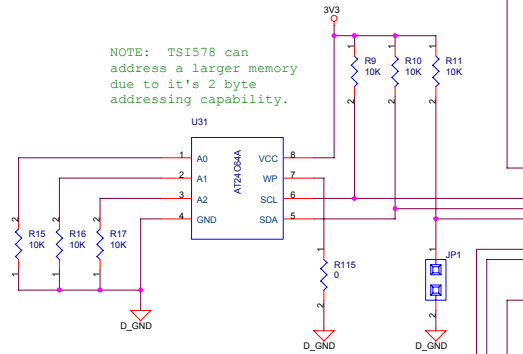
ADDRESS MAP GA[2:0] = UUP

AMC Interface 2		
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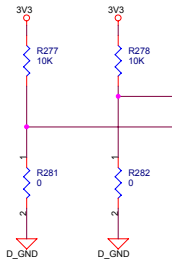
SH [16] TSI578_SPEED1 >> TSI578_SPEED1
 SH [16] TSI578_SPEED0 >> TSI578_SPEED0

NOTE: TSI578 can address a larger memory due to it's 2 byte addressing capability.

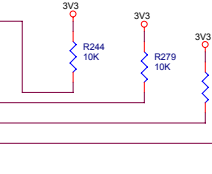
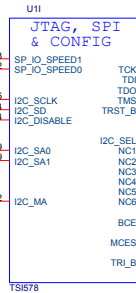


JP1 off - Disable I2C access to external EEPROM
 JP1 on - Enable I2C access to external EEPROM

Select Resistors for I2C Address

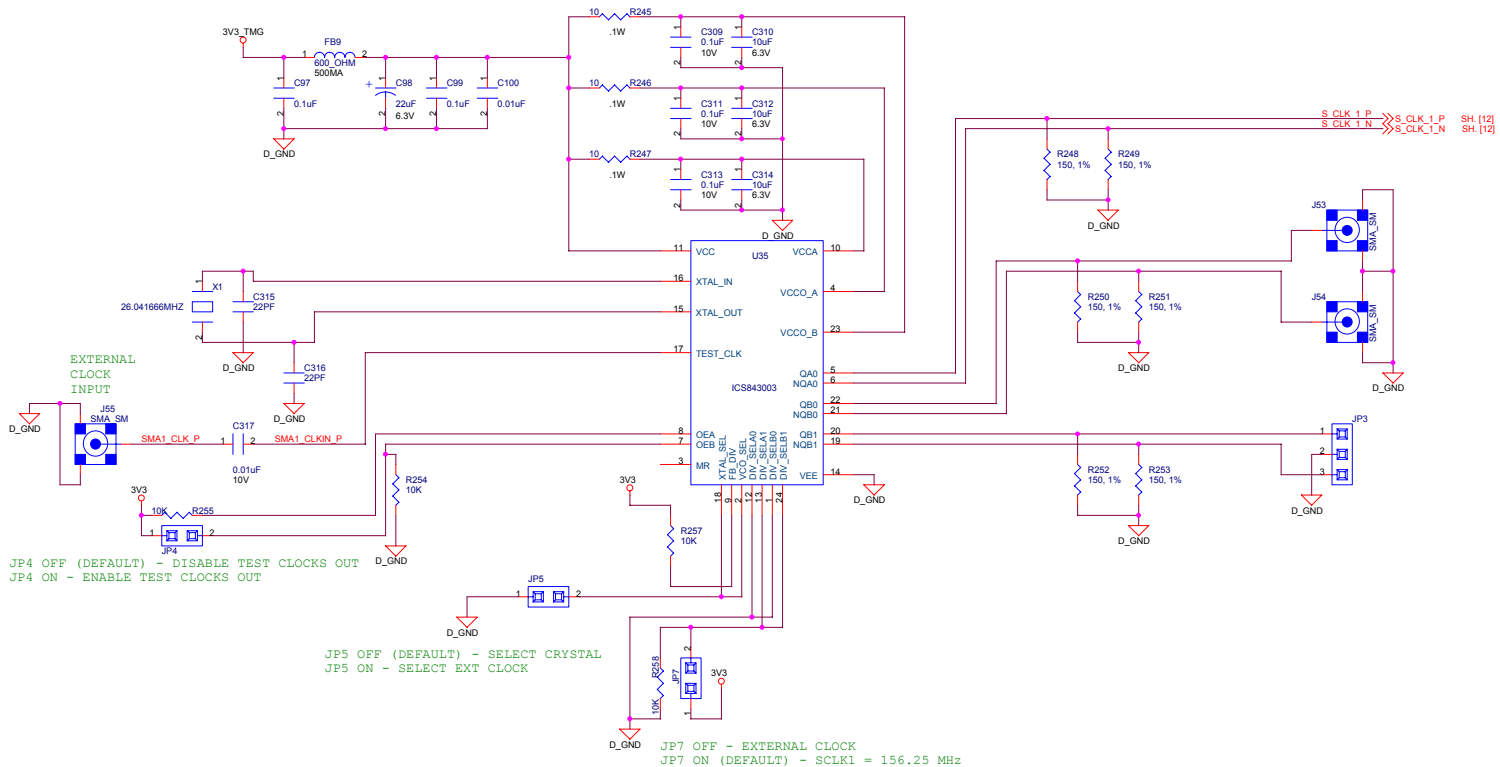


I2C_MA >> I2C_MA



JP11 off - Enable all CMOS pins
 JP11 on - Tri-state all CMOS pins (does not include SERDES or TDO pins)

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EXTERNAL
CLOCK
INPUT

JP4 OFF (DEFAULT) - DISABLE TEST CLOCKS OUT
JP4 ON - ENABLE TEST CLOCKS OUT

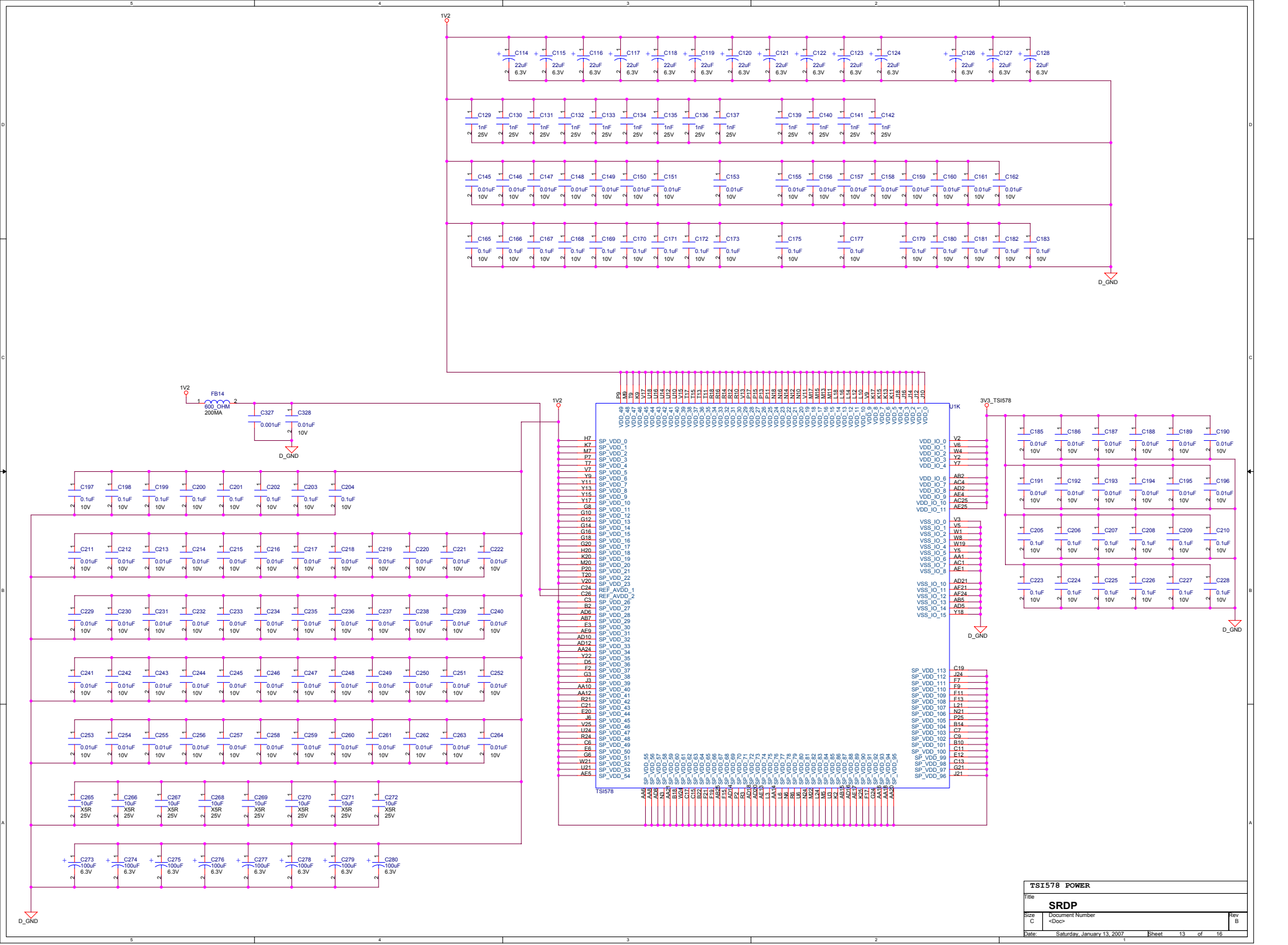
JP5 OFF (DEFAULT) - SELECT CRYSTAL
JP5 ON - SELECT EXT CLOCK

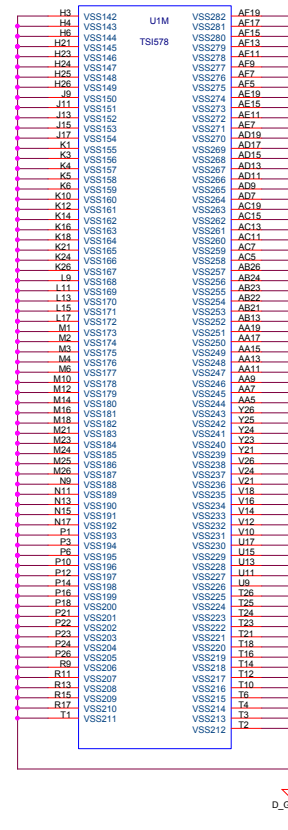
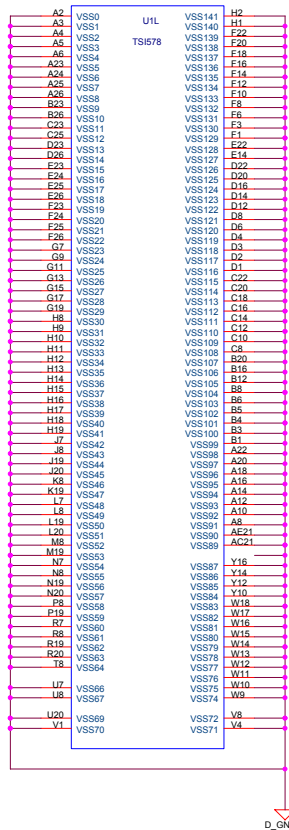
JP7 OFF - EXTERNAL CLOCK
JP7 ON (DEFAULT) - SCLK1 = 156.25 MHz

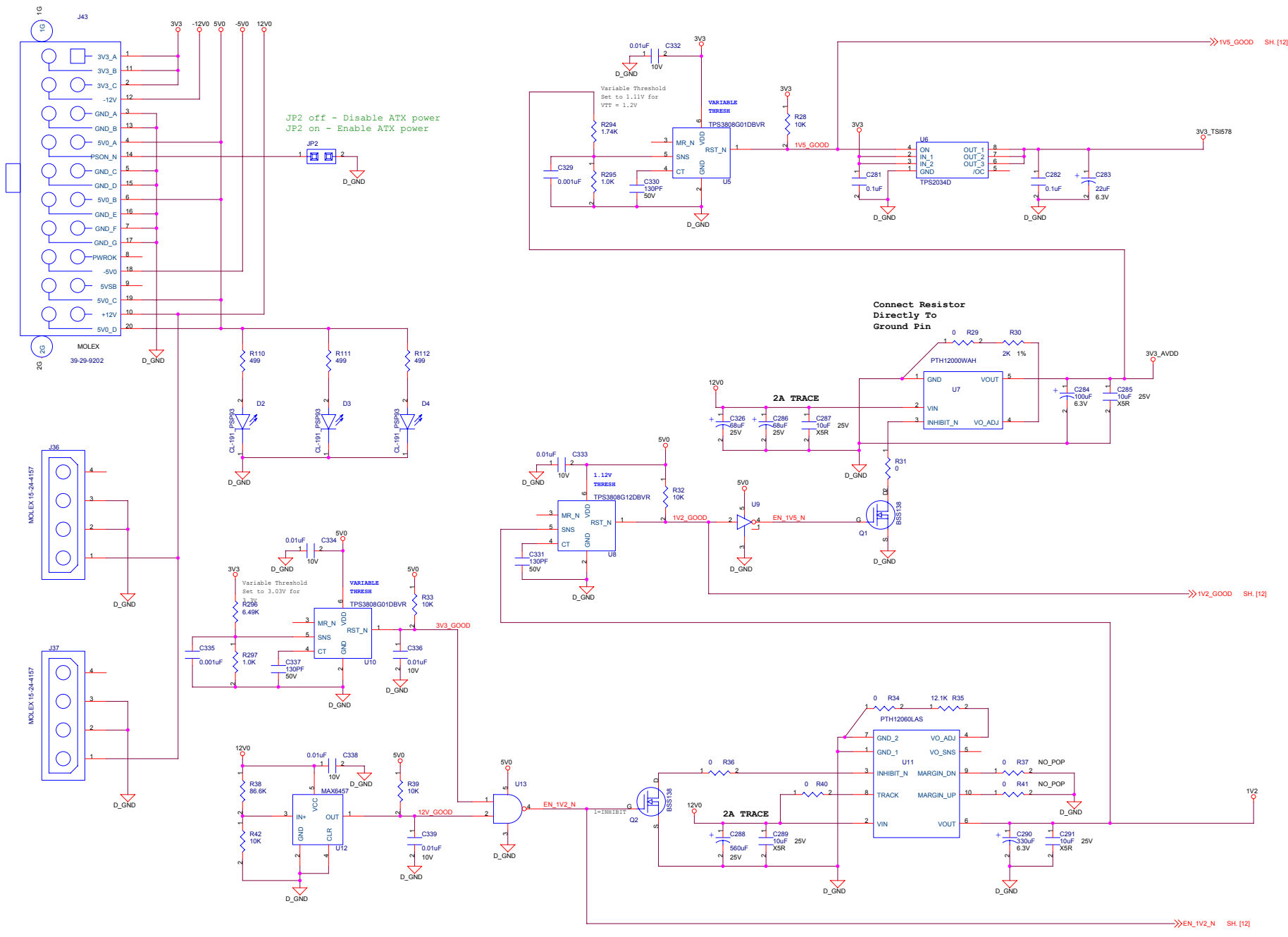
S_CLK_1_P
S_CLK_1_N

SH [12]
SH [12]

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JP2 off - Disable ATX power
 JP2 on - Enable ATX power

Variable Threshold
 Set to 1.11V for
 VTH = 1.2V

Connect Resistor
 Directly To
 Ground Pin

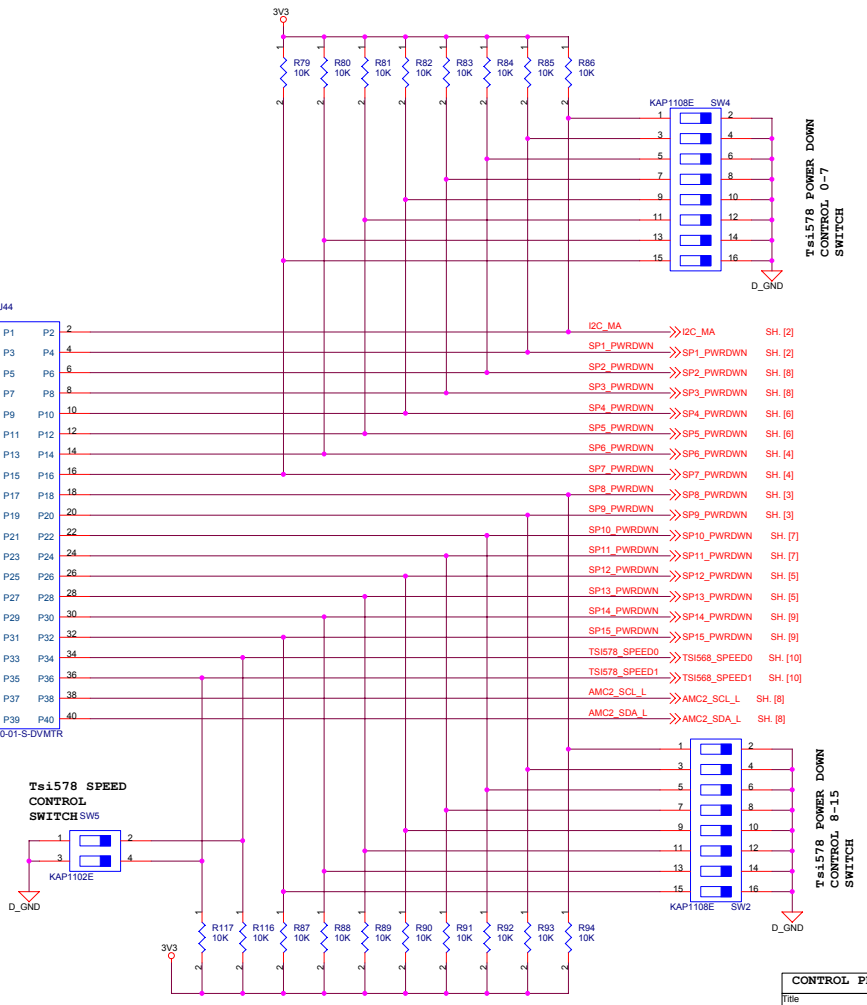
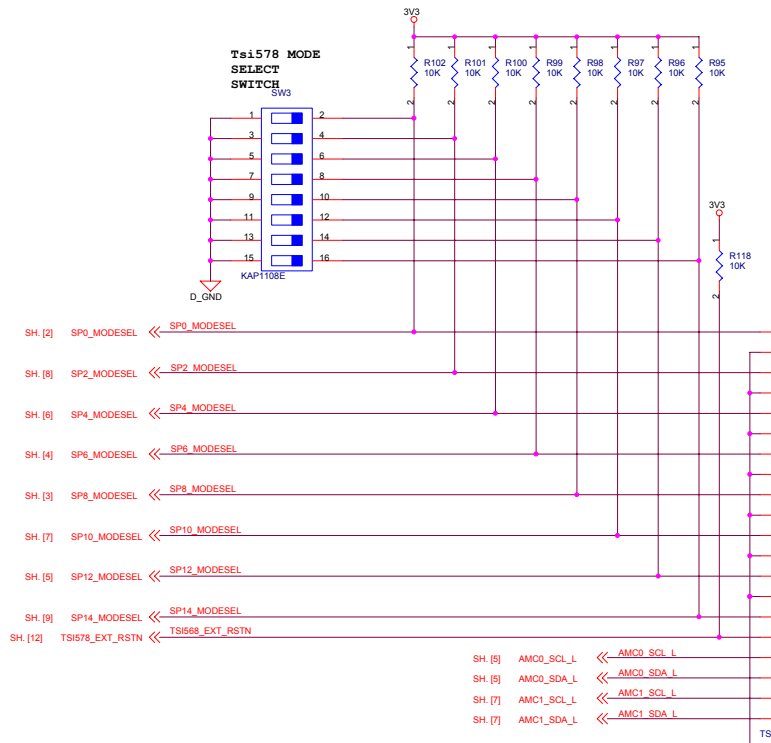
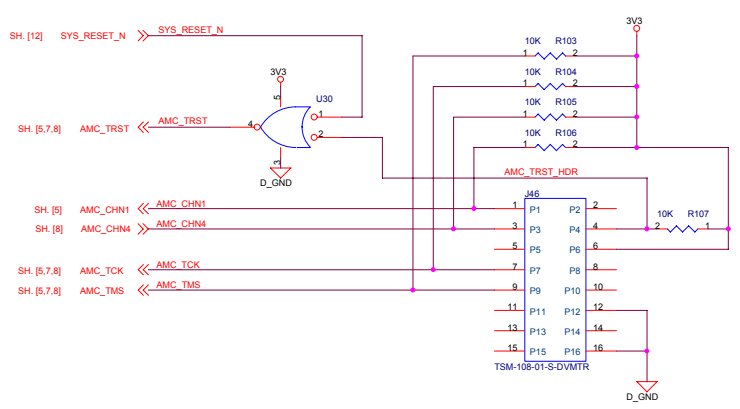
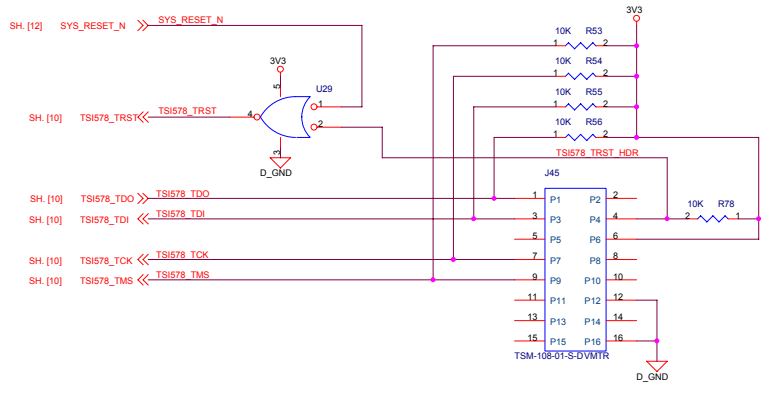
2A TRACE

2A TRACE

POWER CONDITIONING			
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Tsi578 JTAG INTERFACE

AMC JTAG INTERFACE



Tsi578 POWER DOWN CONTROL 0-7 SWITCH

Tsi578 POWER DOWN CONTROL 8-15 SWITCH

CONTROL PROCESSOR INTERFACE

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