

ADS512101 CPLD Revision History

07/18/08

REV	Released	Description
1	03/03/08	CPLD first pass
2	03/13/08	Board ID internal documentation issue (no customer effect)
3	03/17/08	Made changes to BOOT FLASH and BACKUP FLASH access, REG8 Change CPLD reg 16 so default was to enable DVI, VGA, and LVDS interfaces.
4	04/01/08	Add support for ATX power (previously only the barrel connector allowed for power input)
5	04/02/08	ATX power on feature and made more robust (support for really cheap ATX supplies)
6	04/17/08	NAND FLASH disable the CE0 signal now possible
7	04/23/08	PCI interrupts update
8	04/29/08	PCI interrupts update
9	05/15/08	TRST now driven by the assertion of POR
9	05/15/08	Disabled HIB_MODE, excessive battery loading (affects power-up)

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