Silicon Turnkey EXpress

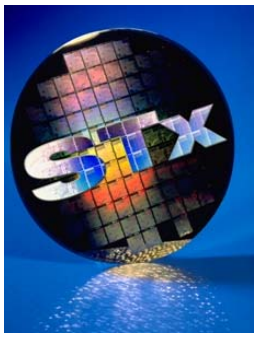
Original Design Manufacturer

P R E L I M I N A R Y

ADS512101

Advanced Development System

User's Manual



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Revision History

Rev	Date	Comments
1.0	Mar 24, 2008	Release of user manual for PCB Rev 3
1.1	Apr 8, 2008	Updated Section 6, Operation, to Rev 3
1.2	Apr 24, 2008	Updated Section 5, CPLD Tables & Section 7.2 Start Up Display, Video Gamma Patch

WARNING: This document is preliminary. It may contain errors and incomplete data. Check with your provider or Silicon Turnkey Express (www.silicontkx.com) or call 440-461-4700) for the latest information.

Support:

Your ADS512101 does include technical support from STx. If you should encounter any start up problems or if the ADS512101 does NOT include all the material, immediately email ADS512101@silicontkx.com and provide your name, contact information and problem. STx commits to acknowledging all requests within 4 hours and usually can resolve most issues within 24 hours.

Additional support information may be found at www.silicontkx.com

Warranty:

To assure all future engineering notifications are communicated the enclosed warranty information must be completed.

NOTICE

The following information is intended to alert the user to possible dangers and important information contained within this guide. The "**WARNINGS**", "**CAUTIONS**" and "**NOTES**" do not eliminate these dangers. Close attention to the information supplied along with "common sense" operation is the major accident prevention measure.

WARNING:	Failure to follow this warning may result in bodily injury.

CAUTION:	Failure to follow this caution may result in possible damage to the board.

NOTE:	Failure to follow this note may result in improper results from the board.

Reference Websites

Below is a list of websites that can be used to obtain additional information and details that may not be fully provided in this manual.

Abatron BDI2000 JTAG Emulator ..... www.ultsol.com/mfgs_emul_abtr.htm
Altera Quartus II…… ...www.altera.com
CodeWarrior USB TAP .....www.freescale.com

5 Volt Only Operation

CAUTION:	Failure to follow this caution may result in possible damage to the board.

The ADS512101 can operate from either 5 VDC only power supplies, such as the 5 watt wall mounted power supply included in this kit, or an ATX standard power supply. When the ADS512101 is operated with the 5W wall mounted power supply included with this kit normal operation will be LIMITED.

5 watt, 5 volts operation will NOT provide 12 volts required for peripherals or PCI. The USB port will NOT provide 500 ma maximum. However all other ADS512101 function will operate nominally.

Other 5 volts power supplies (that meet the specification for the ADS512101) with 7.5 watts or greater will provide support for the maximum USB power of 500 ma. However, 12 volts is NOT supported for peripherals or PCI.

ATX power supplies supports all power for all peripherals and PCI. Follow the instructions in this manual for either 5 volts or ATX operation (see Section 3.2.1).

Media Access Control Address

Every ADS512101 has a unique MAC address saved in memory as part of the standard environment. A label on the backside of the PCB (under the STx logo) provides the PCB revision number, the serial number, and the MAC address. This same information will appear on a label on the CD container.

If the MAC address needs to be reloaded, use these steps:
1 – Boot from main FLASH
2 – Type 'setenv ethaddr ' MAC Address as '00:1E:59:nn:nn:nn'
3 – If an incorrect MAC address is entered, U-Boot must be reloaded and a new MAC address can be entered.

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List of Included Accessories

- User Manual (on CD)
- Schematic (on CD)
- 5V, 5W Wall Mount Power Supply
- Null Modem Cable
- Additional Freescale collateral material (on CD)

List of Optional Accessories

These accessories are available from Silicon Turnkey Express. See the enclosed order form or visit web site:

Accessories

- Cases with custom silkscreen
- Backplates/Custom silkscreen
- LCDs, Inverter, Touchscreen
- Monitors, Touchscreen
- USB 802.11 Radio
- MiniPCI WiMAX Radio
- DRAM Modules
- Memory Upgrades
- Hard Drive (IDE or SATA)
- Solid State Hard Drive (FLASH)
- CD-ROM or DVD Drive
- Wall Cube Power Supplies
- Internal Power Supplies
- PCI Riser Cards
- Peripherals inside the case
- Cables (All kinds & Customs)

Add-On Features

- Bluetooth ® Radio
- Camera/Image Capture
- Microphone
- GPS module
- Echo Cancellation module
- Profibus/Fieldbus

Software

- Operating Systems
- Graphic Solutions
- Cellular Connectivity
- GPS Location
- Touchscreen
- Bluetooth ® Technology
- Voice Recognition
- Wireless
- Database Client

1.0 General Description

The ADS512101 Advanced Development System is a mini-ITX form-factor reference and mother board based on Freescale's MPC5121e microprocessor. The board will provide on-board DDR SDRAM, NOR FLASH, NAND FLASH, (2) 4 wire RS232 ports, 2 CAN ports, USB 2.0, 10/100 Ethernet, Audio in/out/mic, SATA and PATA drive support, PCI, Micro-SD, 24bpp graphics, all powered from a standard ATX or 5 Volt wall mount power supply.

The board can be integrated into any configuration required by the addition of optional peripherals. These would include items such as enclosures, displays, HDD and numerous other mini-ITX accessories.

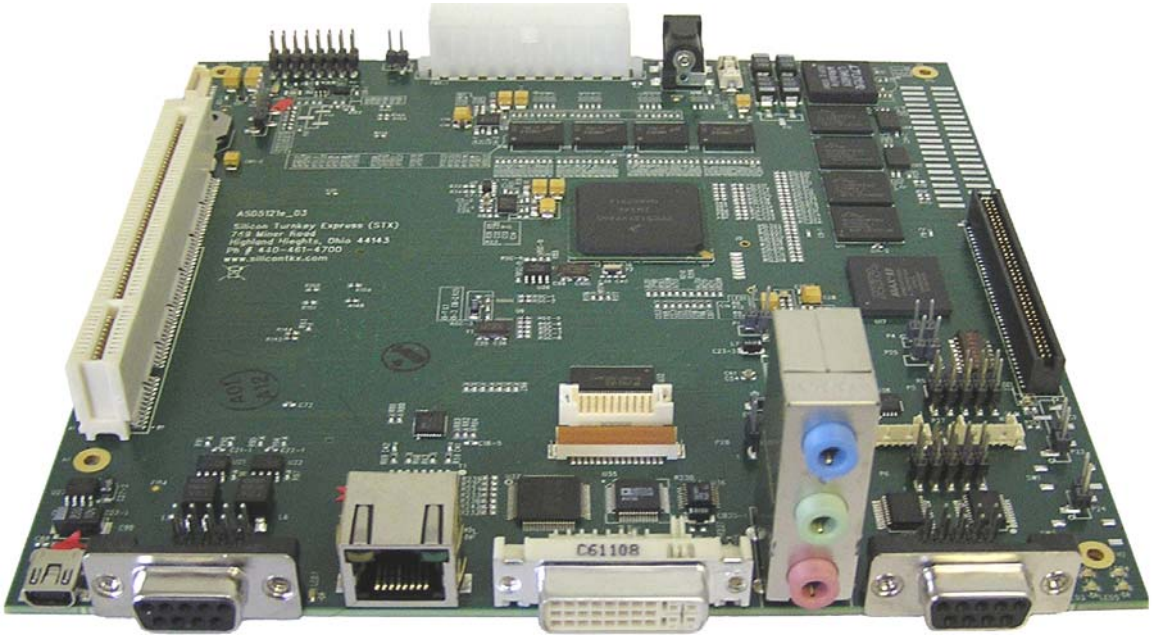


Figure 1 – ADS512101

Silicon Turnkey Express will work with your embedded systems engineers to integrate a final product that will give your end users the best performing and most cost effective embedded solution.

1.1 Device Placement and Functions

This section provides a description of the connectors, jumpers, switches and main components of the ADS512101 board. Refer to Figures 2 and 3 for location of the devices referenced below.

Additional descriptions of the functionality of switches and jumpers along with their recommended settings will be found in Section 3 of this manual.

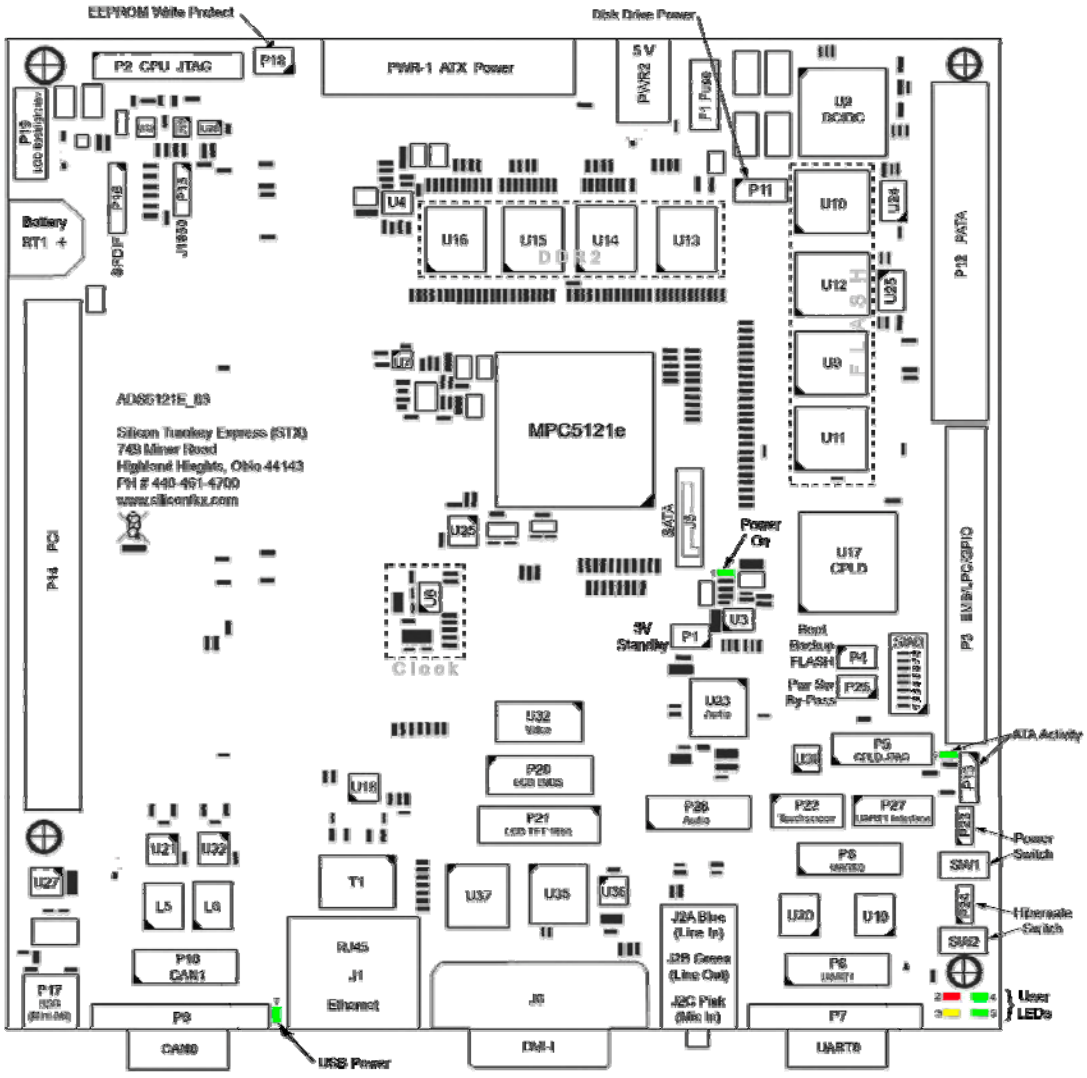


Figure 2 – ADS512101 Top Board Layout

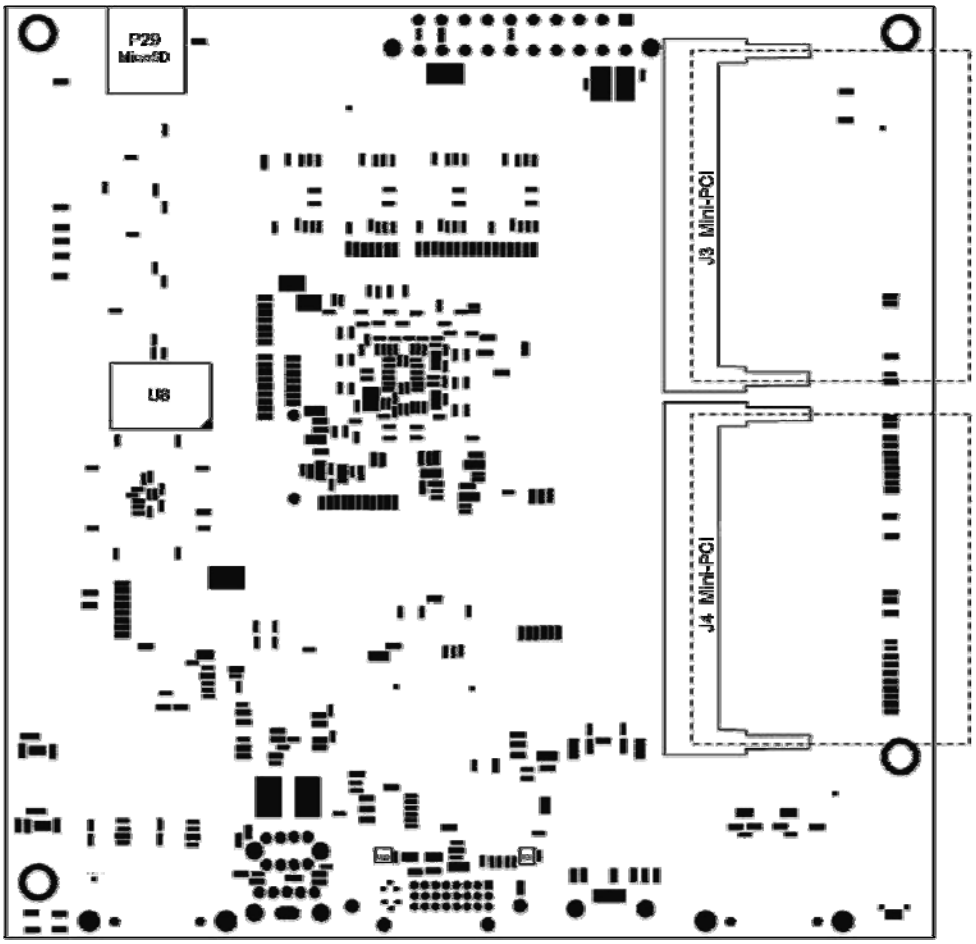


Figure 3 – ADS512101 Bottom Board Layout

1.1.01 BT1 – Battery

Battery type CD2424, 3.3 Volts used for Real Time Clock.

1.1.02 J01 – RJ45, 10/100 BaseT

J1 is a standard Ethernet input jack.

1.1.03 J02 – Audio Connectors

J2 has three stereo connection, J2A (Blue) is Line In; J2B (Green) is Line Out; J2C (Pink) is Aux In.

1.1.04 J03 – Mini-PCI Connector

(See Figure 3)

J3 is a Mini-PCI 32 bit connector with +3.3v that uses ID_SEL_AD22.

1.1.05 J04 – Mini-PCI Connector

(See Figure 3)

J5 is a Mini-PCI 32 bit connector with +3.3v that uses ID_SEL_AD23.

1.1.06 J05 – SATA Interface

J7 is the serial ATA interface connector.

1.1.07 J06 – DVI-I

J24 is the Digital Video Interface.

1.1.08 LED 1 – 5V Good

Indicates when 5 Volts is on.

1.1.09 LED 2 to 5 – CPLD

Is user definable by the CPLD.

1.1.10 LED 6 – ATA Activity

Indicates when ATA data fetches occur.

1.1.11 LED 7 – USB Power

Indicates when USB power is on.

1.1.12 P01 – 5V Only Operation

See Jumpers Section 3.2.6.

1.1.13 P02 – JTAG Connector

Connector P02 is a 16-pin header used for the COP/JTAG input. This port is made available to aid in the programming of the ADS512101.
The pin-outs for the connector are listed in Appendix A

A JTAG interface device, such as the Abatron's BDI2000 or Freescale's CW USB Codetap or equivalent, should be used.

1.1.14 P03 – Expansion Bus

P03 provides signals for EMB, PLC, and GPIO. See Appendix C for pin out.

1.1.15 P04 – Back Up FLASH

Normally Open

A jumper is used to re-FLASH U-Boot to main FLASH. See Appendix XX, Re-FLASH U-Boot.

1.1.16 P05 – CPLD

Header P05 is a CPLD JTAG port for programming and application debugging of the CPLD.

An Altera Quartus II with a Byteblaster cable or equivalent programming kit should be used.

1.1.18 P07 – RS232, UART 0

P7 is a 9-pin "D" style connector for serial communications.

1.1.19 P08 – RS232

P39 is a header connector for an additional RS232 connector. See Appendix B for pin out.

1.1.20 P09 – CAN 0

P9 is a 9-pin "D" style connector for Control Area Network.

1.1.21 P10 – CAN 1

P40 is a header connector for an additional CAN connector. See Appendix B for pin out.

1.1.22 P11 – ATA Drive Select

See Jumper Section 3.2.3.

1.1.23 P12 – PATA Connector

P12 is a 40 pin connector for attaching an optional parallel device.

1.1.24 P13 – Front Panel ATA LED

P13 is a 2-pin header used to enable the front panel LED.

1.1.25 P14 – PCI Connector

J4 is the standard PCI connector that uses ID_SEL_AD21.

1.1.26 P15 – J1850 Interface

P31 is a serial connection for J1850.

1.1.27 P16 – SPDIF Interface

P32 is a connection (header) for the SPDIF to the MPC5121e.

1.1.28 P17 – Mini USB

J23 is a USB mini AB connector that is compatible with the USB 2.0 format.

1.1.29 P18 – EEPROM WP

See Jumper Seciton 3.2.2.

1.1.30 P19 – LCD Backlight Inverter Power

This provides power and control signals to an LCD Inverter.

1.1.31 P20 – LCD Connector

This is a 20 pin LVD connector.

1.1.32 P21 – LCD Connector

This connector is for a TFT, 18bit LCD to accommodate Media5200 monitors.

1.1.34 P22 – Touch Screen Interface

This is an enhancement that may is not available on the standards ADS512101.

1.1.35 P23 – Front Panel Hardware Switch

P26 is a header to provide a connection for the Front Panel Hardware Reset switch SW 1.

Push once (momentary) causes a Power on Reset.

Push and hold for 5 seconds causes a power down.

1.1.35 P24 – Front Panel Hibernation Switch

P27 is a header to provide a connection for the Front Panel Hibernation mode switch SW2.

1.1.36 P25 – Power Switch By-Pass

This jumper is used to by pass the power switch to allow for remote access by applying power to the ADS512101.

1.1.37 P27 – RS232, UART 1

This is a 10 pin header to accommodate an external serial port.

1.1.38 P28 – Audio

This is a 10 pin header to accommodate external audio connections.

1.1.39 P29 – Micro-SD Socket *(See Figure 3)*

P29 allows use of any Micro-SD memory.

1.1.40 PWR-1 – ATX Power Connector

J25 is the main ATX power input connector for the ADS512101. It is designed to use a standard 20-pin ATX power supply.

1.1.41 PWR-2 – DC Power Input

J13 is the 5VDC to the board. P01 needs to be installed to enable the on board power signal. See Section 3.2.6.

1.1.42 SW1 – Power Switch

See Switch Settings, Section 3.1.1

1.1.43 SW2 – Hibernate Switch

See Switch Settings, Section 3.1.2

1.1.44 SW3 – Mode Switch

See Switch Settings, Section 3.1.3

2.0 Hardware Design & Architecture

2.1 General Description

Some of the features of the ADS512101 are:

- Freescale Processor MPC5121e
- DDR2 RAM module- capacity 128Mbyte to 2 Gbytes
- JTAG and control CPLD
- LVDS 24-bit (LCD) or CMOS (Rev3)
- RS-232 and CAN port
- USB A, B and OTG
- NOR, NAND and backup FLASH
- Local bus IO connector
- Stereo Audio (AC97)
- SATA/PATA (IDE), Micro-SD
- PCI/mini-PCI (radio slots)

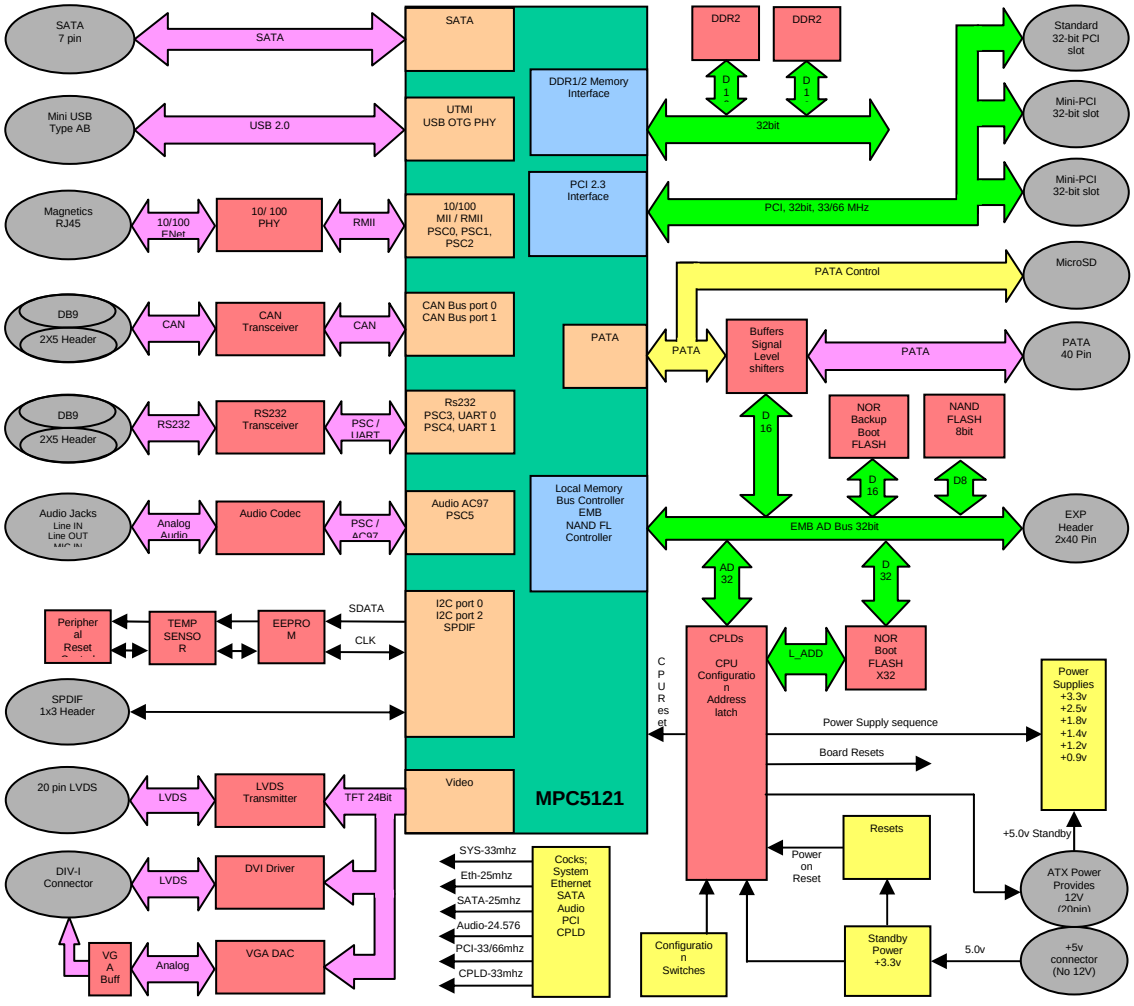


Figure 4- Block Diagram of ADS512101 Board

2.2 Physical Specifications

This section contains general information on the ADS512101's physical characteristics.

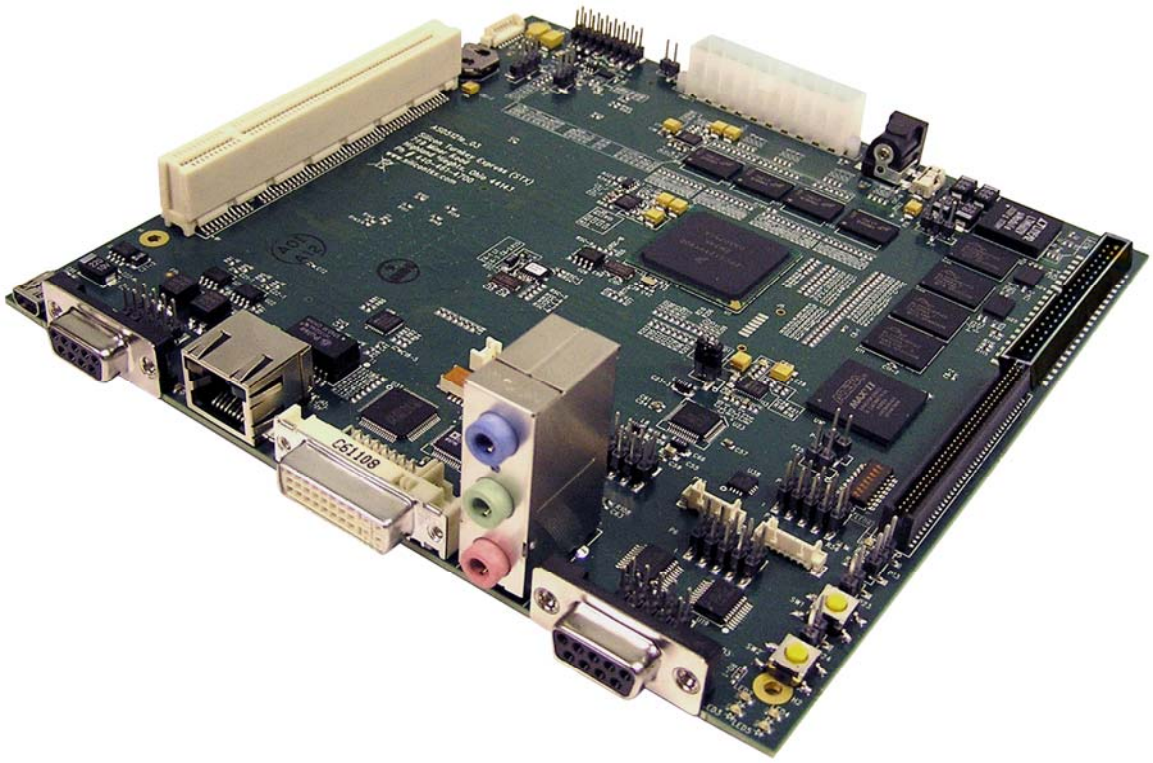


Figure 5 – ADS512101 Side View

Board Size.....mini-ITX (170mm x 170mm)
Power Requirement ..... ATX or 5VDC
Operating Temperature
Standard Version.....0^0 to $+70^0$C
Industrial Version.....-40^0 to $+85^0$C
Weight.....200g
RoHS.....Compliant

3.0 Control & Configuration

This section contains general set-up information about the various jumpers, switches, and LEDs found on the ADS512101 board. Section 3.1 describes the function and recommended switch settings. Section 3.2 describes the function and recommended jumpers on the board. Section 3.3 describes the LED indicator function.

3.1 Switch Settings

This section provides a brief description of the functionality and recommended settings for the switches located on the ADS512101.

Refer to Figure 2 for the locations of these switches.

3.1.1 SW1 – Power On Reset

SW1 is a push button that provides a power on reset signal for the hardware on the ADS512101. The push button can be remotely locate with connector P27.

Push once to power on board and push and hold for five seconds to power down board.

3.1.2 SW2 – Hibernation Mode

SW2 provide a hibernation request to the ADS512101.

Push once to put ADS512101 in hibernation mode. Push again to bring ADS512101 out of hibernation.

3.1.3 SW3 – Boot Mode

CAUTION:	Failure to follow this caution may result in possible damage to the board. For proper operation these switches should be left in the factory default position.

SW3 Boot Mode (Continued)

SW3 is the ***CPLD Boot Configuration Reset functions*** of the ADS512101. Refer to CPLD Register 18, Section 5.19 for additional information.

SW3 is a single-pole single-throw (SPDT) 8-position switch used to configure the CPLD for booting the ADS512101 during power-up.

All switches should be set to factory default, normal operation, 'ON'.

SW	State	Function
1	ON	High Boot
1	OFF	Low Boot
2	ON	NOR Boot
2	OFF	NAND Boot
3	ON	PCI = 33MHz
3	OFF	PCI = 66MHZ*****
4	ON	Watchdog Disabled
4	OFF	Undefined
5	ON	Core PLL = 1.5x
5	OFF	Core PLL = 2x
6-7	ON-ON	DDR2 = 200MHz
6-7	ON-OFF	DDR2 = 166.67MHz
6-7	OFF-ON	DDR2 = 133.33MHz
6-7	ON-ON	DDR2 = 133.33MHz
8	ON	Reserved
8	OFF	Reserved

****M66en must also be high for 66mhz***

3.2 Jumper Settings

This section provides a brief description of the functionality and recommended settings for the jumpers located on the ADS512101. Refer to Figure 2 for the locations of these jumpers.

3.2.1 P01 – ATX Power Supply Operation

Normally Open

This jumper must be installed to use an external 5volt power supply connected to PWR-2. It must be removed to use an ATX power supply.

3.2.2 P04 – Boot Backup FLASH

Normally Open

When this jumper is installed powering the ADS512101 will launch U-Boot in a protected back up FLASH and reinstall U-Boot to main FLASH.

3.2.3 P11 – ATA Drive Voltage Select

CAUTION:	Failure to follow this caution may result in possible damage to the board. Be sure to select the correct voltage setting for the drive used prior to turning the power on to the board.

P11 ATA Drive Voltage Select (Continued)

Normally +3.3 Volts, Pins 1&2

Jumper P21 selects the appropriate power setting (+3.3 or +5.0) per the ATA specification for the drive in use.

Pin No	Description
1	PATA 3V PWR
2	PATA IO PWR
3	PATA 5V PWR

3.2.4 P18 – EEPROM_WP

Normally Open

With this jumper installed the EEPROM can be accessed allowing it to be programmed or erased as needed. When the jumper is removed the EEPROM cannot be programmed.

3.2.5 P25 – Power By-Pass

Normally Open

With this jumper iinstalled the Power On switch is by-passed. The ADS512101 will launch U-Boot when power is applied.

3.3 LED Indicators

This section provides a list of functions for the LEDs on the ADS512101 board. Refer to Figure 2 for the locations of these LEDs.

See CPLD Register 17, Section 5.18, for additional information.

LED	Function	Color
1	5VDC GOOD	GREEN
2	USER DEFINED	RED
3	USER DEFINED	YELLOW
4	USER DEFINED	GREEN
5	USER DEFINED	GREEN
6	ATA ACTIVITY	GREEN
7	USB POWER ON	GREEN

4.0 Schematic

The schematic and basic assembly information in a portable document format for the ADS512101 can be located on the CD in the STx Engineering Document Folder supplied with the board.

The ADS512101 design can be customized for optional flexibility and custom interfaces so the embedded systems engineer can obtain a lower overall parts cost using a variety of fixed and user selectable options.

These options inherently are contained in connectors, jumpers and switches on the board.

The schematic provides guidelines for using the already installed as well as user modifiable options available on the present design.

5.0 CPLD Configuration

The configuration CPLD controls the MPC5121e hard reset configuration word. The hardware configuration is controlled by switches SW3 (see section 3.1.3) and documented in the following CPLD table. If all switches are set to ON, then the CPLD will drive the default configuration word.

Other functions of the CPLD are driven by or read by internal registers that are memory mapped at the base address 0x8200_0000. The CPLD uses the MPC5121e's chip select 2 on the local bus as its chip select and address decodes the lower 5 address bits. See the following table of CPLD registers descriptions for additional information.

5.01 CPLD Register 0

Board ID 1, used along with register 1

Base + 0x00

Bit #	A distinct board ID is assign to the board, 16bits 0x0001 = ADS5121e rev 03	Value at reset	Ability R/ W
7-0	Upper byte of Board ID	0x00	Read only

5.02 CPLD Register 1

Board ID 0, used along with register 0

Base + 0x01

Bit #	Bit description	Value at reset	Ability R/ W
7-0	Upper byte of Board ID	0x03	Read only

5.03 CPLD Register 2

CPLD Revision

Base + 0x02

Bit #	CPLD rev	Value at reset	Ability R/ W
7-0	CPLD rev info Writing a sequence of AA then 55 then 96	0x01	Read only

5.04 CPLD Register 3

Configuration word bits 33..32

Base + 0x03; 0x1010_1000 = default, CPLD drives Reset Configuration Word

Bit #	This register is reserved	Value at reset	Ability R/ W
7-2	Reserved	101010	Read / Write
1	RST_CONF_EMB_AX2	CFG_word_33	Read only
0	RST_CONF_EMB_AX3	CFG_word_32	Read only

5.05 CPLD Register 4

Configuration word bits 31..24

Base + 0x04**;** 0x0000_0001 = default, CPLD drives Reset Configuration Word

Bit #	Ability to read Configuration switches through software Switch definitions are from 5121 user manual HRW	Value at reset	Ability R/ W
7	RST_CONF_SYSDIV, EMB_AX0 driven 0	CFG_word_31	Read only
6	RST_CONF_SYSDIV System PLL divider	CFG_word_30	Read only
5	RST_CONF_SYSDIV	CFG_word_29	Read only
4	RST_CONF_SYSDIV	CFG_word_28	Read only
3	RST_CONF_SYSPLL System PLL Multiply factor	CFG_word_27	Read only
2	RST_CONF_SYSPLL	CFG_word_26	Read only
1	RST_CONF_SYSPLL	CFG_word_25	Read only
0	RST_CONF_SYSPLL	CFG_word_24	Read only

5.06 CPLD Register 5

Configuration switch settings (EMB_AD[23:16])

Base + 0x05; 0x1000_1101 = default, CPLD drives Reset Configuration Word

Bit #	Ability to read Configuration switches by software Switch definitions from 5121 user manual HRW	Value at reset	Ability R/ W
7	RST_CONF_SYSPLL System PLL Multiply factor	CFG_word_23	Read only
6	RST_CONF_CKS_IN Checkstop disabled	CFG_word_23	Read only
5	RST_CONF_NFC_DBW NAND data port 8bit	CFG_word_21	Read only
4	RST_CONF_NFC_PS NAND FLASH page size 2Kbytes	CFG_word_20	Read only
3	RST_CONF_LPC_DBW LPC DATA port 11 =32 bit	CFG_word_19	Read only
2	RST_CONF_LPC_DBW	CFG_word_18	Read only
1	Reserved, not mentioned in manual	CFG_word_17	Read only
0	RST_CONF_LPC_MX LPC Multiplexed mode	CFG_word_16	Read only

5.07 CPLD Register 6

Configuration switch settings (EMB_AD[15:8])

Base **+** 0x06; 0x0101_0000 = default, CPLD drives Reset Configuration Word

Bit #	Ability to read Configuration switches through software Switch definitions are from 5121 user manual HRW	Value at reset	Ability R/ W
7	RST_CONF_PCIARB enable PCI arbiter	CFG_word_15	Read only
6	RST_CONF_PCIHOST PCI Host mode	CFG_word_14	Read only
5	RST_CONF_COREPLL Core PLL Multiply factor	CFG_word_13	Read only
4	RST_CONF_COREPLL Core PLL Multiply factor	CFG_word_12	Read only
3	RST_CONF_COREPLL Core PLL Multiply factor	CFG_word_11	Read only
2	RST_CONF_COREPLL Core PLL Multiply factor	CFG_word_10	Read only
1	RST_CONF_LPC_AX No LPC Address Extension	CFG_word_09	Read only
0	RST_CONF_LPC_AX No LPC Address Extension	CFG_word_08	Read only

5.08 CPLD Register 7

Configuration switch settings (EMB_AD[7:0])

Base + 0x07; 0x0010_0000 = default, CPLD drives Reset Configuration Word

Bit #	Ability to read Configuration switches by software Switch definitions from 5121 user manual HRW	Value at reset	Ability R/ W
7	RST_CONF_PCI66EN M66EN signal, 1 = 66	CFG_word_07	Read only
6	RST_CONF_TLE Little ENDIAN	CFG_word_06	Read only
5	RST_CONF_BMS boot high	CFG_word_05	Read only
4	RST_CONF_COREDIS Core Disable mode (normal)	CFG_word_04	Read only
3	RST_CONF_TPR factory test mode disabled	CFG_word_03	Read only
2	RST_CONF_SWEN watchdog timer disabled at reset	CFG_word_02	Read only
1	RST_CONFIG_ROM_LOC LPC boot	CFG_word_01	Read only
0	RST_CONFIG_ROM_LOC LPC boot	CFG_word_00	Read only

5.09 CPLD Register 8

NOR FLASH Control

Base + 0x08

0x00000000 = default configuration, CPLD drives Reset Configuration Word

Bit #		Value at reset	Ability R/ W
7	Back up FLASH Write Protect 1 = (Full) write protected Write enable signal held high	1	Read / Write
6	Back up FLASH sector write protect	1	Read / Write
5	Boot FLASH Write Protect 1 = (Full) write protected Write enable signal held high	1	Read / Write
4	Boot FLASH sector write protect	1	Read / Write
3	NOR_FL_RDY	1	Read only
2	Boot or Backup FLASH status, 0 = Backup; 1 = Boot Dependant on P4 Jumper, jumper installed = Backup Or if 0xAA is written to register 2, this bit can immediately be written to for software control	x	Read only Read/Write
1	Backup NOR FLASH reset, will be released from reset, at power up, if configuration is set for Backup FLASH	0	Read / Write
0	Boot NOR FLASH reset will be released from reset, at power up, if configuration is set for Backup FLASH	1	Read / Write

5.10 CPLD Register 9

NAND FLASH, CAN, MEDIA_GPIO Control

Base + 0x09

Bit #	Currently only NAND chip select 0 is used, chip select 1-3 are for future expansion.	Value at reset	Ability R/ W
7	MEDIA_GPIO	0	Read only
6	Reserved	0	Read / Write
5	Reserved	0	Read / Write
4	CAN Shut Down 0=Shut Down	0	Read / Write
3	NAND FLASH CE3 # enable 0=enabled	1	Read / Write
2	NAND FLASH CE2 # enable 0=enabled	1	Read / Write
1	NAND FLASH CE1 # enable 0=enabled	1	Read / Write
0	NAND FLASH CE0 # enable 0=enabled	0	Read / Write

5.11 CPLD Register 10

PCI Interrupt Masking

Base + 0x0A

Bit #	1 = interrupt is masked	Value at reset	Ability R/ W
7	PCI_INTB_SLOT3	1	Read / Write
6	PCI_INTA_SLOT3	1	Read / Write
5	PCI_INTB_SLOT2	1	Read / Write
4	PCI_INTA_SLOT2	1	Read / Write
3	PCI_INTD_SLOT1	1	Read / Write
2	PCI_INTC_SLOT1	1	Read / Write
1	PCI_INTB_SLOT1	1	Read / Write
0	PCI_INTA_SLOT1	1	Read / Write

5.12 CPLD Register 11

PCI Interrupt Status

Base + 0x0B

Bit #	PCI interrupts are received at the CPU on the PCI_INTN signal, this is a dedicated input on the CPU, 0=pending, corresponding mask bit also must be cleared	Value at reset	Ability R/ W
7	PCI_INTB_SLOT3	1	Read only
6	PCI_INTA_SLOT3	1	Read only
5	PCI_INTB_SLOT2	1	Read only
4	PCI_INTA_SLOT2	1	Read only
3	PCI_INTD_SLOT1	1	Read only
2	PCI_INTC_SLOT1	1	Read only
1	PCI_INTB_SLOT1	1	Read only
0	PCI_INTA_SLOT1	1	Read only

5.13 CPLD Register 12

Interrupt Routing Selection between CPU IRQ0 or IRQ1

Base + 0x0C

Bit #	Controls which IRQ is used for the listed IRQs 0 = CPU_IRQ0, 1 = CPU_IRQ1	Value at reset	Ability R/ W
7	SW1_HIBERNATE#	0	Read / Write
6	Secure Digital Card (SD_CD#)	0	Read / Write
5	TOUCH_SCR_BUSYN	0	Read / Write
4	TOUCH_SCR_IRQN	0	Read / Write
3	FEC_PHY_INTN	0	Read / Write
2	TEMP_MON_INT	0	Read / Write
1	PCI INTERRUPTS	0	Read / Write
0	Reserved	0	Read / Write

5.14 CPLD Register 13

Interrupt Masking

Base + 0x0D

Bit #	1 = interrupt is masked	Value at reset	Ability R/ W
7	SW1_HIBERNATE#, writing 0 to this bit clears INT in register 14	1	Read / Write
6	Secure Digital Card (SD_CD#)	1	Read / Write
5	TOUCH_SCR_BUSYN	1	Read / Write
4	TOUCH_SCR_IRQN	1	Read / Write
3	FEC_PHY_INTN	1	Read / Write
2	TEMP_MON_INT	1	Read / Write
1	ALL PCI INT MASKING to CPU	1	Read / Write
0	Reserved	1	Read / Write

5.15 CPLD Register 14

Interrupt Status

Base + 0x0E

Bit #	0 = Interrupt pending 0 = pending, corresponding mask bit also must be cleared	Value at reset	Ability R/ W
7	SW1_HIBERNATE#	1	Read only
6	Secure Digital Card (SD_CD#)	1	Read only
5	TOUCH_SCR_BUSYN	1	Read only
4	TOUCH_SCR_IRQN	1	Read only
3	FEC_PHY_INTN	1	Read only
2	TEMP_MON_INT	1	Read only
1	PCI INT, must read CPLD register 11 for which PCI interrupt is asserted	1	Read only
0	Reserved	1	Read only

5.16 CPLD Register 15

MISC Control 0

Base + 0x0F

Bit #		Value at reset	Ability R/ W
7	Reserved	0	Read / Write
6	Reserved	0	Read / Write
5	UART0_FOFF#	1	Read / Write
4	UART1_FOFF# ADS5121e_Rev3.3	1	Read / Write
3	Reserved	1	Read only
2	Reserved	1	Read only
1	PATA_RESET	1	Read only
0	FEC_PHY_RSTN	1	Read only

5.17 PLD Register 16C

Video Control 1

Base + 0x010

Bit #		Value at reset	Ability R/ W
7	LCD_LVDS_FRAME_RATE	0	Read / Write
6	Reserved	0	Read / Write
5	DVI_MSEN	0	Read only
4	LCD_LVDS_SDIRn	0	Read / Write
3	Reserved	0	Read only
2	DVI_DAC_PWRDNn	0	Read only
1	VGA_DAC_PWRDNn	0	Read only
0	LCD_PWR_DWNn	0	Read only

5.18 CPLD Register 17

User LED

Base + 0x011

Bit #		Value at reset	Ability R/ W
7	LED 3 Control, 0=LED0=Reset Status; 1=User Control register 17 (0)	0	Read / Write
6	LED 2 Control, 0=LED0=Reset Status; 1=User Control register 17 (0)	0	Read / Write
5	LED 1 Control, 0=LED0=Reset Status; 1=User Control register 17 (0)	0	Read / Write
4	LED 0 Control, 0=LED0=Reset Status; 1=User Control register 17 (0)	0	Read / Write
3	LED 3	0	Read / Write
2	LED 2	0	Read / Write
1	LED 1	0	Read / Write
0	LED 0	0	Read / Write

5.19 CPLD Register 18

Configuration Switch Settings, SW3

Base + 0x012

Bit #	SW3 Position	Function	Description	Value at reset 0 = OFF	Ability R/W
7	8	Reserved		0	Read only
6-5	7 & 6	cfg_sys_pll	00 = 200mhz DDR2 clock 01 = 166.67mhz DDR2 clock 10 = 133.33mhz DDR2 clock	00	Read only
4	5	cfg_core_pll	0 = 2x 1= 1.5x	0	Read only
3	4	cfg_watchdog	0 = disabled	0	Read only
2	3	cfg_PCI_speed	0 = 33mhz 1 = 66mhz M66en signal also must be high for 66mhz	0	Read only
1	2	cfg_NOR_boot	0 = NOR boot	0	Read only
0	1	cfg_LOW-bo0t	0 = high boot	0	Read only

6.0 Operation

All information contained in this section is from Silicon Turnkey Express' Design Requirements revision 3.2 dated April 7, 2008. For additional information or clarifications contact Silicon Turnkey Express or email ADS512101@silicontkx.com.

6.1 Central Processing Unit

The ADS512101's MPC5121e is configured to run with a 33 MHz system clock, and asynchronous mode 66 MHz/33 MHz PCI clock frequency. The initial configuration is from the main CPLD which reads the configuration of switch SW3. The boot strap options will be selectable from a configuration dip switch read by the CPLD, the actual boot strap pins will be driven by the CPLD during reset only. The switch setting can also be read from the CPLD, see CPLD register 18.

The MPC5121e is responsible for the PCI arbitration and interrupt controller.

The MCP5121e provides the interface to local on board resources including: NOR FLASH memory, NAND FLASH memory, DDR2-SDRAM memory, CPLD, MII (10/100 Fast Ethernet Controller), I2C (EEPROM, STM), PSC (programmable serial controller) for RS232 and AC97 (audio), Interrupt controller, USB 2.0 (ULPI), PCI bus, PCI controller, Graphics (on chip MBX) controller, PATA controller, SATA controller and Micro-SD.

See MPC5121e user manual for detail descriptions for each interface.

6.2 Power supplies

The ADS512101 board requires a mini-ATX power supply (20 pins connector) or a +5v external power supply. When using a +5v external power supply functions requiring +12v will not operate. If a +5v external power supply is used jumper P1 is required. The jumper connects the +5v with the +5v_stby voltage which is required for the power up circuitry.

CAUTION:	It is NOT recommended to power on with both the ATX and +5v external power supply installed.

6.2.1 Power Rails

The ADS512101 board requires several power rails that are provided on board, and include:

Power Rails (continued)

+1.4v @ TBD for the CPU Core voltage.
+1.2v @ 0.5A for the CPU Core voltage.
+1.8v @ 4A for the CPU Core voltage.
+0.9v @ 3.3A for the CPU Core voltage.
+3.3v @ 2.0A for the CPLD, reset circuitry, clocks. CPU I/O, and peripheral logic.
+12v @ 2A (direct input from off-board power supply) for disk drive power and LCD.

6.2.2 Power Sequencing

The CPLD is responsible for enabling all of the power rails except the +3.3v_stby power. The +3.3v_stby power is enabled constantly. Power sequencing follows rules for the MPC5121e which requires IO voltage rail to be powered before the Core Voltages. Power sequencing is accomplished with daisy chained regulators. Starting when +3.3v reaches 90% of its output, a power good signal occurs and enables the next power regulator. Several different power on modes exist and defined by CPLD configurations.

ATX Power Supply sequencing starts when SW1 is actuated providing a signal to the CPLD. Counters determine the actuation time of SW1. If the actuation time is longer than 3 seconds, atx_off_cntr times out and all power is disabled. A momentary actuation generates a Power On Reset.

Power sequencing using a +5v external power supply is the same as for the ATX Power Supply sequencing, except the CPLD senses when an external power supply is used and will not enable the ATX supply.

Immediate power on sequencing for either an ATX or external power supply can be enable by installing jumper P25. With the P25 jumper installed SW1 will only generate a Power ON Reset.

6.2.3 Hibernation Mode

Although the hibernate circuit has completed design, it has not been fully implemented or tested. Contact Silicon Turnkey Express for more details or email questions to ADS512101@silicontkx.com.

Hibernate uses SW2 and can be used as an interrupt to the MPC5121e, see registers 12-14 in section 5.13 to 5.15. The hibernate signal from the MPC5121e will shut down all of the regulators and devices. Hibernate can wake or sleep per the MPC5121e specification.

For controlled entry into the hibernate mode, the MPC5121e must be prepared in anticipation of entering the hibernate mode, that is, having the power supply removed. The CPU must first write a value to the time target register that will give the MPC5121e enough time to complete all bus transactions in progress. The CPU terminates any other processes in an orderly manner. Then the MPC5121e enters the hibernation mode before the HIB_MODE pin is asserted which will turn off the external power sources. (See section 9.4.3 of the MPC5121e user manual.)

6.2.3 Hibernation Mode (continued)

The external signals SET_WU_SRC[0:5] are used as external wakeup signals. (See section 9.2 of the MPC5121E user manual.)

GPIO 30 is used to initiate hibernation or wake from hibernation mode.

6.3 Resets

Power On Reset (POR) is derived from the power supervisor circuit.

POR circuitry monitors the power supplies and will output the RST_POR# signal if any of the power rails fall below their trip points (+1.4v; +1.8v; +3.3v).

The CPLD drives the RST_MASTER# signal to the POR circuitry's manual reset input and will generate a Power On Reset. The CPLD can drive this signal based on the following:

- SW1 actuation
- CPLD register 2 written sequence: 0xAA, 0x55, 0x96
- MPC5121e hard and soft resets are generated by the CPLD and are just 'OR' with JTAG hard and soft reset along with the Power On Reset.

6.7 Clocks

The main clock driver is a programmable clock synthesizer IC (Cypress CY22392).

CLK_E_SYS is the main processor clock (33.33 MHz). The CLK_E_CPLD (33.33 MHz) is used by the CPLD for synchronization to the CPU's input clock and internal functions.

CLK_B_CPLD_.5E is used by the CPLD and is one half the CLK_E_CPLD frequency and will be 16.66 MHz.

CLK_A_USB is used by the CPU's internal USB circuitry and is 24.00 MHz.

CLK_FETH_CPU is used by both the CPU's internal fast Ethernet circuitry and the Ethernet PHY, CLK_FETH_PHY and is 25.00 MHz.

CLK_D_SATA is used by the CPU's internal SATA drive circuitry and is 25.00 MHz.

CPLD_CLK_BASIC is used by the CPLD for internal functions.

CLK_C_24.576mhz_B is used by the Audio Codec circuitry.

6.7 CPU Configuration

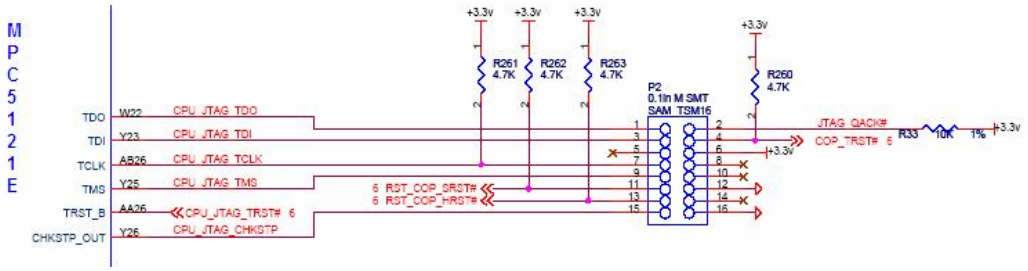
The MPC5121e configuration is selectable by SW3 and can be read from the CPLD register 18, see section 5.19. All 32 configuration signals are driven by the CPLD during power on reset only. The MPC5121e configuration status is read from the CPLD registers 3 to 7, see sections 5.04 to 5.08.

Default configuration: see table 7-3 Reset Configuration Word in the MPC5121e user manual.

Bit [0..31] = 0000_0111_00??_??11_0?10_110?_????_????
Bit [1..0] = RST_CONF_ROMLOC = 00 = LPC boot.
Bit 2 = RST_CONF_SWEN = 0 = watchdog timer at reset disabled.
Bit 3 = RST_CONF_TPR = 0 = Factory test mode (normal operation).
Bit 4 = RST_CONF_COREDIS = 0 = Core disable mode (normal operation.
Bit 5 = RST_CONF_BMS = 1 = boot mode select,
set so ROM loc start address = 0xFF80.
Bit 6 = RST_CONF_TLE = 1 = little endian mode.
Bit 7 = RST_CONF_PCI66EN = 1 = PCI66Mhz operation.
Bit [9 & 8] = RST_CONF_LPC_AX = 00 = no LPC address extension.
Bit [13 to 10] = RST_CONF_COREPLL = TBD.
Bit 14 = RST_CONF_PCIHOST = 1 = PCI host mode.
Bit 15 = RST_CONF_PCIARB = 1 PCI arbiter enabled.
Bit 16 = RST_CONF_LPC_MX = 0 = LPC non-multiplex mode.
Bit 17 = not describe in user manual. This may be used for LPC_AX3?
For the switch function.
Bit [19 & 18] = RST_CONF_LPC_DBW = 01 = LPC data port size = 16 bit.
Bit 20 = RST_CONF_NFC_PS = 1 = NAND FLASH page size = 2k page size.
Bit 21 = RST_CONF_NFC_DBW = 1 = NAND FLASH 8 bit data port size.
Bit 22 = RST_CONF_CKS_IN = 0 = checkstop input disabled.
Bit [26 to 23] = RST_CONF_SYSPLL = TBD.
Bit [LPC_AX3, 31 to 27] = RST_CONF_SYSDIV = TBD.

6.6 JTAG Port

The JTAG port is configured as a standard Freescale COP port and will accept most debug tools.



6.7 Interrupts

The MPC5121e has 2 interrupt sources; CPU_IRQ0 and CPU_IRQ1.

The IPIC can receive 56 separate interrupts from different interrupt domains as follows:

- 2 external—off-chip interrupt signals sources are IRQ[1:0]
- 57 internal—on-chip interrupt signals sources are: DDR MEMC, LPC, NFC, PATA, PCI, DMA, MU, FEC, PSC, FIFOC, USB, CSB arbiter, CAN, BDLC, DIU, AXE, SPDIF, SDHC, RTC, GTM, I2C, GPIO, GPT, SATA, MBX, TEMP, IIM and PMC.
- 1 external and 5 internal—off-chip interrupt signal source is IRQ0. On-chip MCP interrupt signals sources are software watchdog timer (WDT), PCI, temperature sensor and system bus arbiter (SBA)

The CPLD accepts all other on board interrupts, and multiplexes these interrupts onto the MPC5121e's IRQ signals. These will be user selectable, TBD.

PCI_SLO_INTA#;	PCI_SLO_INTB#;	PCI_SLO_INTC#A;	PCI_SLO_INTD#;
PCI_SL1_INTA#;	PCI_SL1_INTB#;	PCI_SL2_INTA#;	PCI_SL2_INTB#;
FEC_PHY_INT#;	RTC_INT#;	TEMP_IRO#;	TOUCH_IRO#;
TOUCH_BUSY#;	PCI_CPU_INT#;	SW1_HIBERNATE#	

6.8 Memory

6.8.1 DDR2 SDRAM

The dedicated DDR2 memory bus is a 32 bits data, single bank, 256 Mbytes Max @ 200 MHz, no ECC. It uses the MPC5121e DDR2 SDRAM controller and is directly connection to the MPC5121e.

6.8.2 NOR FLASH

The FLASH memory is 64 Mbytes total, 16 bits wide, and its interface consists of 3 devices; 2 banks of main FLASH and 1 bank of BOOT Flash. The FLASH uses the chip select LPC_CS0#. This chip select is connected to the CPLD, and the CPLD directs the appropriate NOR_FLx_CSN signal to the correct FLASH.

6.8.3 NAND FLASH

Dedicated NAND FLASH memory can be up to 2 GB, 8 bits wide and directly connected to the MPC5121e.

6.9 I/O Function

See Appendix B for pin definitions

6.9.01 10/100 Ethernet, J1

The 10/100 Ethernet port uses the Freescale MPC5121e MII interface and a standard RJ45 connector with indicator LEDs and a 10/100 Ethernet PHY. The Port 0 PHY address is 00001.

6.9.02 RS232 / RS485 Port (4-wire) P06 to P08

Two PSC (programmable serial controller) ports can be configured as UART, RS232, 4 wire port. The PSC is configured within the MPC5121e, see user MPC5121e manual for details on setting up PSC. Transceivers are directly connected to a 9 pin D, DB9 connector and a 10 pin header.

6.9.03 CAN BUS, P09 & P10

Two Individual Controller Area Network Buses are a 2 wire interface used mainly by the automotive industry. The CAN specification defines the Data Link Layer; ISO 11898 defines the Physical Layer. The CAN bus [CAN bus] is a balanced (differential) 2-wire interface running over either a Shielded Twisted Pair (STP), Un-shielded Twisted Pair (UTP), or Ribbon cable. Each node is connected to a male 9 pin D connector and a 10 pin header. The Bit Encoding used is: Non Return to Zero (*NRZ*) encoding (with bit-stuffing) for data communication on a differential two wire bus. The use of NRZ encoding ensures compact messages with a minimum number of transitions and high resilience to external disturbance.

Both CAN buses are directly connected to the MPC5121e's dedicated CAN bus and use transceivers which are connected to a 9 pin D, DB9 connector and a 10 pin header.

6.9.04 I2C Bus

Two I2C ports use Port 0 and Port 2.

Port 0 (I2C0) is used for:

- Serial EEPROM with address set to binary 1, 0, 1, 0, A2, A1, A0, R/W, or 0xA0.
- Temperature monitor with address set to binary 1, 0, 0, 1, A2, A1, A0, R/W, or 0x92.
- RTC with address hard coded at 0xD0. A battery backup is provided and is automatically switched within the device. The RTC provides a square wave output:
  CLK_RTC is connected to the CPLD>

I2C Bus (continued)

Port 2 (I2C2) is used for:

- Digital potentiometer with address is hard coded to 0x5C.
- Digital Transmitter with address is set to 0x70 read, 0x71 write.

6.9.07 USB 2.0, P17

The USB 2.0 Host port is connected directly to MPC5121e dedicated USB 2.0 controller. A USB power switch is used to turn on and off the USB power. USB control and fault condition controlled directly from MPC5121e.

6.9.06 AUDIO and Touch Screen controller, J02 & P22

The MPC5121e use a PSC (programmable serial controller) set for the AC97 communication protocol. The audio codec is controlled by the AC97 controller and provides LINE IN, LINEOUT and MIC IN.

The Touch Screen controller is population option and not available on the standard ADS512101. Contact ADS512101@silicontkx.com for information.

6.9.07 VIDEO, J06, P20, P21

The MPC5121e has an integrated graphics engine, the PowerVR® MBX Lite IP core. The MBX controller is directly connected to:

- A 24-bit LVDS transceiver.
- A Triple 8 bit video DAC with whose output is high speed video buffered then connected to the DVI-I connector.
- A Digital transmitter that is connected to the DVI-I connector.

6.9.08 LCD Backlight, P19

The LCD backlight uses a digital potentiometer to control the LCD backlight and is controlled directly from the MPC5121e's I2C interface and addressed at 0x5C.

6.9.09 SATA Drive Interface, J05

The MPC5121e directly connects to the SATA drive connector.

6.9.10 PATA Drive Interface, P12

The PATA Interface has been disabled and may prevent the ADS512101 from booting, if the voltage jumper select, P11, is installed.

The PATA drive circuitry uses the MPC5121e PATA bus interface which is connects to signal level translator ICs to convert from the MPC5121e's +3.3v signal level to the PATA +5.0v signal level. The level translated signals are then connected to the PATA connector.

6.9.10 PATA Drive Interface (continued)

The PATA power is selectable by jumper P11, either +3.3v or +5v. PATA power, +12v, is supplied directly from the ATX power connector.

6.9.11 PCI, P14

The PCI slot is compliant to PCI2.3, 32 bit bus. It can either be 33 MHz or 66 MHz which is determined by selectable clock with the Mode Switch, SW3. This is 3.3 volts only.

6.9.12 Mini-PCI, J3 & J4

Two Mini-PCI slots are compliant to PCI2.3, 32 bit bus. It can either 33 MHz or 66 MHz which is determined by selectable clock with the Mode Switch, SW3. This is 3.3 volts only.

6.9.13 Micro-SD, P29

A Micro-SD slot is available and is directly connected to the MPC5121e ATA controller.

7.0 U-Boot

7.1 Standard Commands

```
?       - alias for 'help"
asknev  - get environment variables from stdin
autoscr - run script from memory
base    - print or set address offset
bdinfo  - print Board Infro structure
boot    - boot default, i.e., run 'bootcmd'
bootd   - boot default, i.e., run 'bootcmd'
bootm   - boot application image from memory
bootp   - boot image via network using BootP/TFTP protocol
clocks  - print clock configuration
cmp     - memory compare
coninfo - print console devices and information
cp      - memory copy
crc32   - checksum calculation
dhcp    - invoke DHCP client to obtain IP/boot params
echo    - echo args to console
erase   - erase FLASH memory
exit    - exit script
flinfo  - print FLASH memory information
go      - start application at address 'addr'
help    - print online help
i2c     - I2C sub-system
icrc32  - checksum calculation
iloop   - infinite loop on address range
imd     - i2c memory display
iminfo  - print header information for application image
imls    - list all images found in flash
imm     - i2c memory modify (auto-incrmenting)
imw     - memory write (fill)
inm     - memory modify (constant address)
iprobe  - probe to discover valid I2C chip addresses
itest   - return true/false on integer compare
loadb   - load binary file over serial line (Kermit mode)
loads   - load S-Record file over serial line
loady   - load binary file over serial line (ymodem mode)
loop    - infinite loop on address range
md      - memory display
mii     - MII utility commands
mm      - memory modify (auto-incrementing)
mtest   - simple RAM test
mw      - memory write (fill)
nfs     - boot image via network using NFS protocol
nm      - memory modify (constant address)
ping    - send ICMP ECHO_REQUEST to network host
printenv - print environment variables
protect - enable or disable FLASH write protection
rarpboot - boot image via network using RARP/TFTP protocol
reset   - Perform RESET of the CPU
run     - run commands in an environment variable
saveenv - save environment variables to persistent storage
setenv  - set environment variables
sleep   - delay execution for some time
test    - minimal test like /bin/sh
tftpboot - boot image via network using TFTP protocol
version - print monitor verison
```

7.2 Start Up Display

```
U-Boot 1.3.2 (Mar 14 2008 - 12:42:04) MPC512X

CPU:   MPC5121e rev. 1.0, Core e300c4 at 399.999 MHz, CSB at 199 MHz
Board: ADS5121 rev. 0x0301 (CPLD rev. 0x02)
I2C:   ready
DRAM:  512 MB
FLASH: 64 MB
*** Warning - bad CRC, using default environment

PCI:   Bus Dev VenId DevId Class Int
In:    serial
Out:   serial
Err:   serial
Net:   FEC ETHERNET

Type "run jffs2boot" to boot Linux

Hit any key to stop autoboot:  0
=>
```

Figure 6 – U-Boot Start Screen

7.2.1 U-Boot Warnings

```
*** Warning - bad CRC, using default environment
```

This indicates a new U-Boot has been started and environment variables have not been saved. To eliminate this warning, a 'saveenv' command must be performed.

7.2.2 Auto Linux Boot

If Freescale's Linux has been pre-loaded in the ADS512101, it will auto boot from U-Boot. The following information will appear after U-Boot runs:

```
Type "run jffs2boot" to boot Linux
Hit any key to stop autoboot:  0
Usage:
cp      - memory copy

## Booting image at ffc40000 ...
```

If you do NOT want Linux to boot hold down any key after U-Boot is running.

Linux takes several minutes to load and boot. Linux is operating when the command line prompt appears:

Linux Prompt: **-sh-2.05b#**

7.2.3 Graphic Demonstration
(Spinning Vehicle)

A demonstration program may be loaded in your ADS512101. This program can be launched by typing after the Linux prompt: 'demoloop'. This program has been provided by Freescale to demonstrated the graphics capability of the MPC5121e.

7.2.4 Video Gamma LTIB Patch

The ADS512101 only works in two video modes. A command has been patched in Freescale's LTIB that will enable either mode of operation. The command changes the number of color bits that drive the video output modes.

Default enables the DVI (J6) output for correct color information. In the default mode both the LVDS (P20) and TFT (P21) will not output the correct color information.

To enable both the LVDS video out and TFT video out a command has to executed at the Linux prompt as follows:

gamma_set LCD

To switch back to DVI video output, default mode, execute at the Linux prompt:

gamma_set

Not all ADS512101 with LTIB loaded may have this patch included. Complete instructions and patch are available from Silicon Turnkey Express. Either call sale at 440.461.4700 ext 182 or email ADS512101@silicontkx.com for information.

7.3 Re-Install U-Boot Instructions

The ADS512101 has a protected back up FLASH memory for U-Boot. If U-Boot should become corrupt for any reason, U-Boot can be re-installed. Please follow these instructions to re-flash U-Boot to the main memory.

1 – Remove power from the ADS512101

2 – Install a jumper on the 'Back Up Flash' Header, P4

3 – Reconnect power to the ADS5121 and use SW1 to launch U-Boot.

– This process will write the back up U-Boot to main memory.

– Follow the on screen instructions.

4 – Remove power from the ADS512101

5 – Remove the jumper from header P4.

6 – Reconnect power to the ADS512101 and use SW1 to launch U-Boot.

Re-install U-Boot display:

```
U-Boot 1.3.2 (Mar 14 2008 - 12:42:04) MPC512X

CPU:   MPC5121e rev. 1.0, Core e300c4 at 399.999 MHz, CSB at 199 MHz
Board: ADS5121 rev. 0x0301 (CPLD rev. 0x02)
I2C:   ready
DRAM:  512 MB
FLASH: 64 MB
PCI:   Bus Dev VenId DevId Class Int
In:    serial
Out:   serial
Err:   serial
Net:   FEC ETHERNET

BOOTING FROM BACKUP FLASH
RECOVERY MODE PROCESS STARTING at AUTOBOOT ...
Hit any key to stop autoboot:  0
Copying U-Boot image to dram
Switching to main flash and erasing
Un-Protected 1 sectors

. done
Erased 1 sectors
PROGRAMMING MAIN FLASH with U-BOOT IMAGE
Copy to Flash... done

PLEASE SELECT MAIN FLASH BY REMOVING JUMPER at P4

Rebooting in 10 Seconds
Resetting the board.
```

Figure 7 –U-Boot Re-Installing Screen

8.0 Linux

8.1 Freescale's Linux BSP

For current versions of Freescale's Linux visit www.freescale.com.

```
Linux BSP for Freescale MPC5121EADS
Beta Release 20071210

This is a release of the Freescale Semiconductor MPC5121EADS Linux BSP.
This BSP has been tested and all features are believed to be functioning
correctly except as noted in this document.  If you find an issue, please
report it to www.freescale.com for validation.

The following hardware is supported:

  MPC5121e processor on the ADS5121 platform.
  For configuration information, please see
  /Help/software/User_Manual_ADS5121_LTIB_BSP.pdf
  on the BSP CD image.

=========================================================
MPC5121eADS BSP FEATURES
=========================================================

Linux Kernel Info:
    * Linux-2.6.22 kernel

Beta Linux BSP Supported Devices
    * Serial UART (PSC)
    * Fast Ethernet Controller (FEC)
    * PATA (Upto UDMA3)
    * Display Interface Unit (DIU)
    * On board ST M41T00 RTC (not on chip RTC)
    * USB Host (Full Speed only)
    * NOR Flash
    * NFC NAND Flash controller
    * SPI (PSC)
    * Direct Memory Access (DMA)
    * AC97

U-Boot version 1.2.0 + Patches

Toolchain info
    *  Toolchain components:
       o binutils-2.17 + CodeSourcery patches.
       o gcc-4.1.2 + CodeSourcery patches.
       o eglibc-2.5.59
       o linux 2.6.21 sanitized kernel headers.
       o gdb-6.6.50.20070424-cvs + CodeSourcery patches (not included)

    * Toolchain target: powerpc-e300c3-linux-gnu
       o Hence the prefix for all toolchain executables is: powerpc-
         e300c3-linux- for example: powerpc-e300c3-linux-gnu-gcc

    * Toolchain prefix: /opt/freescale/usr/local/gcc-4.1.69-eglibc-2.5.69-
      1/powerpc-e300c3-linux-gnu

GDB 6.3.50 (from LTIB)

Package List (default)


=========================================================
KNOWN ISSUES
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ADS Board Errata
ISSUE:  Some boards require HW mods for proper operation of
        Audio, NAND and USB.
WORKAROUND:  See summary in help/hardware/SummaryofADSErrata.pdf.

PATA
ISSUE:  The on board level shifters are not powered on be default.
```

```
WORKAROUND:  See instructions in the PATA Doc.

DIU
ISSUE:  DVI transmitter is not enabled in u-boot by default.
WORKROUND:   To enable the DVI transmitter issue the following commands in
             u-boot before booting the linux kernel:
             i2c dev 2
             i2c mw 38 8.1 bf 1

ISSUE:  There is a conflict between DIU and DMA in hardware causing
        underruns that hang the DIU.
WORKAROUND:  None

USB
ISSUE:  Bug #872. (Host mode) High speed devices do not work reliably.
ISSUE:  Bug #872. (Host mode) Sometimes the device is unusable when a
        device is connected after the driver is loaded, the following
        message is displayed: over-current change on port 1
ISSUE:  Bug #872. (Device mode) USB bus resets received from the host
        cause the 5121 to hang.
WORAROUND:   See the USB Doc for workarounds.

AUDIO
ISSUE:  Bug #892. There is a 10 second delay after an audio file finishes
        playing
WORKAROUND:  None

ISSUE:  Bug #938. The audio driver does not play mono wave files.
WORKAROUND:  None

ISSUE:  Some boards require HW mods for audio to function.
WORKAROUND:  See ADS Board Errata above.

ISSUE:  Bugs #949, #961, #962. Audio quality degrades with high ethernet
        traffic.
        This includes playing audio with mplayer from a server or madplay
        over nfsroot or madplay from PATA drive.
WORKAROUND:  None

ISSUE:  Bug #917. Playing wav audio file with gstreamer is sometimes
        garbled.
WORKAROUNG:  None

ISSUE:  Bug #955. Playing mp3 audio with gstreamer playbin fails.
WORKAROUNG:  None

FEC
ISSUE:  Bug #895. The FEC driver does not function correctly if the FEC is
        not initialized by u-boot.  This happens with a JFFS2 deploy.
WORKAROUND:  Issue a ping command in u-boot before doing a jffs2boot.

AXE
ISSUE:  Bug #964. Running the sample axe client application axec
        repeatedly will eventually cause the memory allocator in the
        driver to fail.
WORKAROUND:  Avoid doing this.

ISSUE:  Bug #963. The axe driver can only be loaded once per reboot.  The
        current axe driver does not put the axe hardware into reset state
        on unload so loading the driver a second time fails.
WORKAROUND:  To restart the axe driver you need to reboot.

FLASHIMAGE
ISSUE:  Bug #953.  The binary flash image on the iso only boots to the u-
        boot prompt.
        User input is needed to boot all
```

8.2 Linux Auto Boot Display:

```
## Booting image at ffc40000 ...
   Image Name:   Linux-2.6.22
   Created:      2008-03-12  13:18:46 UTC
   Image Type:   PowerPC Linux Kernel Image (gzip compressed)
   Data Size:    1626758 Bytes =  1.6 MB
   Load Address: 00000000
   Entry Point:  00000000
   Verifying Checksum ... OK
   Uncompressing Kernel Image ... OK
   Booting using the fdt at 0xffec0000
   Loading Device Tree to 007fc000, end 007fefff ... OK
Unable to update property /soc@80000000:bus-frequency, err=FDT_ERR_NOTFOUND
Unable to update property /soc@80000000/ethernet@2800:local-mac-address, err=FDT_ERR_NOTFOUND
Using MPC5121 ADS machine description
Linux version 2.6.22 (root@r21893-11-linux) (gcc version 4.1.2) #7 Wed Mar 12 08:18:42 CDT 2008
preallocate_diu_videomemory: diu_size=5242880
preallocate_diu_videomemory: diu_mem=c1c00000
MPC5121 ADS board from Freescale Semiconductor
Zone PFN ranges:
  DMA             0 ->    65536
  Normal      65536 ->    65536
early_node_map[1] active PFN ranges
    0:        0 ->    65536
Built 1 zonelists.  Total pages: 65024
Kernel command line: console=ttyPSC0,115200 root=/dev/mtdblock1 rw rootfstype=jffs2 mem=256M
IPIC (128 IRQ sources) at fdffec00
PID hash table entries: 1024 (order: 10, 4096 bytes)
Dentry cache hash table entries: 32768 (order: 5, 131072 bytes)
Inode-cache hash table entries: 16384 (order: 4, 65536 bytes)
Memory: 226560k/262144k available (3208k kernel code, 35428k reserved, 128k data, 111k bss, 160k init)
Mount-cache hash table entries: 512
NET: Registered protocol family 16
Could not initialize clk mbx_clk without a calc routine
Could not initialize clk spdif_txclk without a calc routine
Could not initialize clk spdif_rxclk without a calc routine
PCI: Probing PCI hardware
Generic PHY: Registered new driver
SCSI subsystem initialized
usbcore: registered new interface driver usbfs
usbcore: registered new interface driver hub
usbcore: registered new device driver usb
NET: Registered protocol family 2
IP route cache hash table entries: 2048 (order: 1, 8192 bytes)
TCP established hash table entries: 8192 (order: 4, 65536 bytes)
TCP bind hash table entries: 8192 (order: 3, 32768 bytes)
TCP: Hash tables configured (established 8192 bind 8192)
TCP reno registered
JFFS2 version 2.2. (NAND) © 2001-2006 Red Hat, Inc.
io scheduler noop registered
io scheduler anticipatory registered (default)
io scheduler deadline registered
io scheduler cfq registered
MBX IRQ: 66
fb0: DISP0 Panel0 fb device registered successfully.
FSL-DIU-FB: registed FB device driver!
Serial: MPC512x PSC UART driver
80011300.serial: ttyPSC0 at MMIO 0x80011300 (irq = 40) is a MPC52xx PSC
RAMDISK driver initialized: 16 RAM disks of 32768K size 1024 blocksize
loop: module loaded
fs_enet.c:v1.0 (Aug 8, 2005)
FEC MII Bus: probed
Uniform Multi-Platform E-IDE driver Revision: 7.00alpha2
ide: Assuming 50MHz system bus speed for PIO modes; override with idebus=xx
MPC512X: IDE driver, (c) 2004-2007 Freescale Semiconductor
```

```
__fsl_ata_resetproc: resetting ATA controller
Freescale(R) MPC5121 DMA Engine found, 64 channels
fsldma: Self-test copy successfully
hda: no response (status = 0xa1), resetting drive
hda: no response (status = 0xa1)
hdb: no response (status = 0xa1), resetting drive
hdb: no response (status = 0xa1)
fc000000.flash: Found 2 x16 devices at 0x0 in 32-bit bank
 Amd/Fujitsu Extended Query Table at 0x0040
fc000000.flash: CFI does not contain boot bank location. Assuming top.
number of CFI chips: 1
cfi_cmdset_0002: Disabling erase-suspend-program due to code brokenness.
RedBoot partition parsing not available
physmap-flash fc000000.flash: Using OF partition information
Creating 5 MTD partitions on "fc000000.flash":
0x00000000-0x00040000 : "protected"
0x00040000-0x03c40000 : "filesystem"
0x03c40000-0x03ec0000 : "kernel"
0x03ec0000-0x03f00000 : "device-tree"
0x03f00000-0x04000000 : "u-boot"
No NAND device found!!!
fsl-ehci fsl-ehci.0: Found HC with no IRQ. Check fsl-ehci.0 setup!
Initializing USB Mass Storage driver...
usbcore: registered new interface driver usb-storage
USB Mass Storage support registered.
usbcore: registered new interface driver libusual
Freescale High-Speed USB SOC Device Controller driver (Apr 20, 2007)
Can't find OTG driver!
mice: PS/2 mouse device common for all mice
i2c /dev entries driver
usbcore: registered new interface driver usbhid
drivers/hid/usbhid/hid-core.c: v2.6:USB HID core driver
Advanced Linux Sound Architecture Driver Version 1.0.14 (Thu May 31 09:03:25 2007 UTC).
ALSA device list:
  #0: mpc512x-ac97 (National Semiconductor LM4550)
TCP cubic registered
NET: Registered protocol family 1
NET: Registered protocol family 17
drivers/rtc/hctosys.c: unable to open rtc device (rtc0)
VFS: Mounted root (jffs2 filesystem).
Freeing unused kernel memory: 160k init
Setting the hostname to freescale
Mounting filesystems
Starting syslogd and klogd
Starting inetd:
pvr: module license 'Proprietary.' taints kernel.
__ioremap(): phys addr 0x500000 is RAM lr d106e764
CLCDC_Init: major device 252
================================================================================
* MBX Driver, ALT Software Inc.                                                 *
* Build 04, February 13, 2008                                                   *
================================================================================
DIU Framebuffer start:                0x 1c08000
DIU Framebuffer virtual:              0xc1c08000
DIU Framebuffer size:                 3145728 bytes
MBX Render data start:                 0x  500000
================================================================================
bits_per_pixel:    32
width:            1024
height:           768
red.length:        8
green.length:      8
blue.length:       8
__ioremap(): phys addr 0x1900000 is RAM lr d5097b00
Continuing to load PowerVR services
Loaded PowerVR consumer services.
-sh-2.05b#
```

Appendix A – Memory Map

The following memory map isonly an example, refer to the MCP5121e user manual for specific memory map configurations, many of these memory map settings are user defined.

Function	**Bytes**	**32 Bit Address**		**CS#**	**Size**
	Reserved	**Start**	**End**		
IMMRBAR Default setting at reset FF40 0000 Move after boot		8000 0000	803F FFFF		1M Recommend. 4M For future revs
DDR SDRAM	256MB	0x0000 0000	0x0FFF FFFF	DDR_MCSN	256MB
BOOT Space EBC NOR FLASH Boot High	64MB	0xFC00 0000	0xFFFF FFFF	LPC_CS0N	64MB
NAND FLASH Upto 2GB	1MB	0x4000 0000	0x400F FFFF		1MB
PCI Memory PCILAWBAR0-2	256MB 256MB 256MB 256MB	0xA000 0000 0xB000 0000 0xC000 0000 0xD000 0000	0xAFFF FFFF 0xBFFF FFFF 0xCFFF FFFF 0xDFFF FFFF		1GB
SRAM	256KB	0x3000 0000	0x3001 FFFF		128KB
CPLD	32B	0x8200 0000	0x820F FFFF	LPC_CS2N	32B
MBX (graphics)	16MB	0x2000 0000	0x20FF FFFF		16MB
USB ULPI 2.0 Device	4KB	IMMR_0x3000	IMMR_3FFF		4KB
PATA Drive		IMMR_0x1 0200	IMMR_0x1 02FF		
SATA Drive		IMMR_0x2 0000	IMMR_0x2 1FFF		
Local Configuration Registers	1KB	IMMR_0x0 0000	IMMR_0xF FFFF		64B
RS232 A	PSC3	IMMR_0x1 1300	IMMR_0x1 13FF		
RS232 B	PSC4	IMMR_0x1 1400	IMMR_0x1 14FF		
Audio (AC97)	PSC5	IMMR_0x1 1500	IMMR_0x1 15FF		
CAN A		IMMR_0x0 1300	IMMR_0x0 137F		
CAN B		IMMR_0x0 1380	IMMR_0x0 13FF		
IIC0		IMMR_0x0 1700	IMMR_0x0 171F		32B
IIC2		IMMR_0x0 1740	IMMR_0x0 17FF		32B
Fast Ethernet Controller		IMMR_0x0 2800	IMMR_0x0 2FFF		256B

Appendix B – Connector Pin Assignments

J01 – Ethernet

Pin No	Description
1	TCT
2	TDP
3	TDN
4	RDP
5	RDN
6	RCT
7	LD1C
8	LD1A
9	LD2C
10	LD2A
1G	G1
2G	G2

J02– Audio Jack

Pin No	Description
1	SHIELD GND
J2C	Microphone
2	RIGHT MIC 2 (OUTER)
3	AGND
4	LEFT MIC 1 (INNER)
5	AGND
J2B	Line Out
22	RIGHT HP OUT (OUTER)
23	AGND
24	LEFT HP OUT (INNER)
25	AGND
J2A	Line In
32	RIGHT LINE IN (OUTER)
33	AGND
34	LEFT LINE IN (INNER)
35	AGND

J3/J4 – Mini PCI 2/3

Pin No	Description
1	TIP
2	RNG
3	8PMJ3
4	8PMJ1
5	8PMJ6
6	8PMJ2

J3/J4 – Mini PCI 2/3 continued

Pin No	Description
7	8PMJ7
8	8PMJ4
9	8PMJ8
10	8PMJ5
11	LED1P
12	LED2P
13	LED1N
14	LED2N
15	CHSGND
16	Reserved1
17	(not)INTB
18	5V1
19	3.3V1
20	(not)INTA
21	Reserved2
22	Reserved3
23	GND1
24	3.3VAUX1
25	CLK
26	(not)RST
27	GND2
28	3.3V2
29	(not)REQ
30	(not)GNT
31	3.3V3
32	GND3
33	AD31
34	(not)PME
35	AD29
36	Reserved4
37	GND4
38	AD30
39	AD27
40	3.3V4
41	AD25
42	AD28
43	RSVD5
44	AD26
45	C (not)BE3
46	AD24
47	AD23
48	IDSEL

J3/J4 – Mini PCI 2/3 continued

Pin No	Description
49	3.3V5
50	GND6
51	AD21
52	AD22
53	AD19
54	AD20
55	GND7
56	PAR
57	AD17
58	AD18
59	C (not)BE2
60	AD16
61	(not)IRDY
62	GND8
63	3.3V6
64	(not)FRAME
65	(not)CLKRUN
66	(not)TRDY
67	(not)SERR
68	(not)STOP
69	GND9
70	3.3V7
71	PERR N
72	(not)DEVSEL
73	C (not)BE1
74	GND10
75	AD14
76	AD15
77	GND11
78	AD13
79	AD12
80	AD11
81	AD10
82	GND12
83	GND13
84	AD9
85	AD8
86	C (not)BE0
87	AD7
88	3.3V8
89	3.3V9
90	AD6
91	AD5
92	AD4
93	Reserved6

J3/J4 – Mini PCI 2/3 continued

Pin No	Description
94	AD2
95	AD3
96	AD0
97	5V2
98	Reserved WIP1
99	AD1
100	Reserved WIP2
101	GND14
102	GND15
103	AC SYNC
104	(not)M66E
105	AC SDIN
106	AC SDOUT
107	AC BCLK
108	AC CODEC IO
109	AC CODECID1
110	(not)AC RESET
111	MOD AUDIO MON
112	Reserved7
113	AUDIO GND1
114	GND16
115	AUDIO OUT
116	AUDIO IN
117	AOUT GND
118	AIN GND
119	AUDIO GND2
120	AUDIO GND3
121	Reserved8
122	(not)MPCIACT
123	5VANA
124	3.3VAUX2

J06 – DVI-I

Pin No	Description
C1	ANALOG RED
C2	ANALOG GRN
C3	ANALOG BLUE
C4	ANALOG H-SYNC
C5_1	ANALOG RTN1
C5_2	ANALOG RTN2
1	TX2-
2	TX2+
3	TX2/4 SHLD
4	TX4-

J06 – DVI-I continued

Pin No	Description
5	TX4+
6	DDC CLK
7	DDC DATA
8	ANALOG V-SYNC
9	TX1-
10	TX1+
11	TX1/3 SHLD
12	TX3-
13	TX3+
14	5VDC
15	GND
16	TX0-
17	HP DETECT
18	TX0+
19	TX0/5 SHLD
20	TX5-
21	TX5+
22	TSC SHLD
23	TXC+
24	TXC-
25	SHELL1
26	SHELL2

P02 – MPC5121e JTAG

(16 pin Header)

Pin No	Description
1	5121E JTAG COP TDO
2	5121E JTAG COP QACKN
3	5121E JTAG COP TDI
4	COP CON TRSTN
5	TP110 JTAG COP HALTED
6	3.3VDC
7	5121E JTAG COP TCK
8	NC
9	5121E JTAG COP TMS
10	NC
11	SOFT RESET N
12	GND
13	HARD RESET N
14	NC
15	5121 CPU CHKSTP OUT
16	GND

P03 – Expansion Bus

Pin No	Description
1	GND
2	GND
3	EMB AD0
4	EMB AD1
5	EMB AD2
6	EMB AD3
7	EMB AD4
8	EMB AD5
9	EMB AD6
10	EMB AD7
11	3.3VDC
12	3.3VDC
13	EMB AD8
14	EMB AD9
15	EMB AD10
16	EMB AD11
17	EMB AD12
18	EMB AD13
19	EMB AD14
20	EMB AD15
21	GND
22	GND
23	EMB AD16
24	EMB AD17
25	EMB AD18
26	EMB AD19
27	EMB AD20
28	EMB AD21
29	EMB AD22
30	EMB AD23
31	3.3VDC
32	3.3VDC
33	EMB AD24
34	EMB AD25
35	EMB AD26
36	EMB AD27
37	EMB AD28
38	EMB AD29
39	EMB AD30
40	EMB AD31

P03 – Expansion Bus continued

Pin No	Description
41	GND
42	GND
43	LPC CS2N
44	EMB AX3
45	LPC ACKN
46	EMB AX2
47	LPC OEN
48	EMB AX1
49	LPC R WN
50	EMB AX0
51	PWR ON RESET N
52	TP117
53	HARD RESET N
54	TP118
55	GND
56	TIP116
57	LPC CLK
58	TP119
59	GND
60	GND
61	CPU GPIO14
62	TP115
63	CPU GPIO15
64	TP120
65	CPU GPIO28
66	TP114
67	CPU GPIO29
68	TP121
69	CPU GPIO30
70	TP113
71	CPU GPIO31
72	TP112
73	3.3VDC
74	3.3VDC
75	TP123
76	TP111
77	TP122
78	TP109
79	GND
80	GND

P05 – CPLD JTAG

(10 pin Header)

Pin No	Description
1	CPLD_TCK
2	GND
3	CPLD_TDO
4	5V_STANDBY
5	CPLD_TMS
6	NC
7	NC
8	NC
9	CPLD_TDI
10	GND

P06 – UART 0

(10 pin Header)

Pin No	Description
1	NC
2	CSER PB RXD
3	CSER PB TXD
4	NC
5	GND
6	NC
7	CSER PB RTS
8	CSER PB CTS
9	NC
10	NC

P07 – UART 0

Pin No	Description
1	TP003
2	CSER PA RXD
3	CSER PA TXD
4	TP005
5	GND
6	TP004
7	CSER PA RTS
8	CSER PA CTS
9	TP006

P08 – UART 1

(10 pin Header)

Pin No	Description
1	NC
2	CSER PB RXD
3	CSER PB TXD
4	NC
5	GND
6	NC
7	CSER PB RTS
8	CSER PB CTS
9	NC
10	NC
Pin No	Description
1	TP011

P09 – CAN 0

Pin No	Description
1	TP011
2	CANL
3	GND
4	TP014
5	SIG GND
6	TP012
7	CANH
8	TP013
9	TP015

P10 – CAN 1

(10 pin Header)

Pin No	Description
1	NC
2	CANL
3	GND
4	NC
5	SIG GND
6	NC
7	CANH
8	NC
9	NC
10	NC

P12 – PATA Connector

Pin No	Description
1	PATA CON RESET
2	GND
3	PATA CON AD7
4	PATA CON AD98
5	PATA CON AD6
6	PATA CON AD9
7	PATA CON AD5
8	PATA CON AD10
9	PATA CON AD4
10	PATA CON AD11
11	PATA CON AD3
12	PATA CON AD12
13	PATA CON AD2
14	PATA CON AD13
15	PATA CON AD1
16	PATA CON AD14
17	PATA CON AD0
18	PATA CON AD15
19	GND
20	NC
21	PATA CON DRQ
22	GND
23	PATA CON IOWN
24	GND
25	PATA CON IORN
26	GND
27	PATA CON IOCHRDY
28	GND
29	PATA CON DACK
30	GND
31	PATA CON INTRQ
32	PATA CON IOCS16N
33	PATA CON DA1
34	NC
35	PATA CON DA0
36	PATA CON DA2
37	PATA CON CS0N
38	PATA CON CS1N
39	PATA CON DASPN
40	GND

P13 – ATA Activity

(2 pin Header)

Pin No	Pin Name
1	SIGNAL (PATA IO PWR + PATA CON DASPN
2	GND

P14 – PCI

Pin No	Pin Name
B1	-12V
A1	(not)TRST
B2	TCK
A2	12V
B3	GND0
A3	TMS
B4	TDO
A4	TDI
B5	5V 1
A5	5V
B6	5V 2
A6	(not)INTA
B7	(not)INTB
A7	(not)INTC
B8	(not)INTD
A8	5V 5
B9	(not)PRSNT1
A9	Reserved3
B10	Reserved1
A10	3.3V (I/O)
B11	(not)PRSNT2
A11	Reserved4
B12	--
A12	--
B13	--
A13	--
B14	Reserved2
A14	3.3v (AUX)
B15	GND1
A15	(not)RST
B16	CLK
A16	3.3V (I/O) 3
B17	GND2
A17	GNT
B18	(not)REQ
A18	GND9
B19	3.3V (I/O) 1
A19	(not)PME

P14 – PCI continued

Pin No	Pin Name
B20	AD31
A20	AD30
21B	AD29
A21	3.3V 7
B22	GND19
A22	AD28
B23	AD27
A23	AD26
B24	AD25
A24	GND10
B25	3.3V 1
A25	AD24
B26	C/(not)BE3
A26	IDSEL
B27	AD23
A27	3.3V 8
B28	GND20
A28	AD22
B29	AD21
A29	AD20
N30	AD19
A30	GND11
B31	3.3V 2
A31	AD18
B32	AD17
A32	AD16
B33	C/(not)BE2
A33	3.3V 9
B34	GND3
A34	(not)FRAME
B35	(not)IRDY
A35	GND12
B36	3.3V 3
A36	(not)TRDY
B37	(not)DEVSEL
A37	GND13
B38	GND4
A38	(not)STOP
B39	(not)LOCK
A39	3.3V 10
B40	(not)PERR
A40	Reserved5
B41	3.3V 4
A41	Reserved6
B42	(not)SERR

P14 – PCI continued

Pin No	Pin Name
A42	GND14
B43	3.3V 5
A43	PAR
B44	C/(not)BE1
A44	AD15
B45	AD14
A45	3.3V 11
B46	GND5
A46	AD13
B47	AD12
A47	AD11
B48	AD10
A48	GND15
B49	M66EN
A49	AD09
B50	GND6
A50	GND16
B51	GND7
A51	GND17
B52	AD08
A52	C/(not)BE0
B53	AD07
A53	3.3V 12
B54	3.3V 6
A54	AD06
B55	AD05
A55	AD04
B56	AD03
A56	GND18
B57	GND8
A57	AD02
B58	AD01
A58	AD00
B59	3.3V (I/O) 2
A59	3.3 (I/O) 4
B60	(not)ACK64
A60	(not)REQ64
B61	5V 3
A61	5V 6
B62	5V 4
A62	5V 7

P15 – J1850

(3 pin Header)

Pin No	Pin Name
1	CPU J1850 TX
2	CPU J1850 RX
3	GND

P16 – SPDIF

(4 pin Header)

Pin No	Pin Name
1	SPDIF TXCLK
2	SPDIF TX
3	SPDIF RX
4	GND

P17 – USB Mini AB Connector

Pin No	Pin Name
1	USB CONMB PWR
2	USB CONMB DN
3	USB CONMB DP
4	USB CONMB ID
5	GND
6	SHIELD GND
7	SHIELD GND
8	SHIELD GND
9	SHIELD GND

P19 – LCD Backlight

Pin No	Pin Name
1	12VDC
2	12VDC
3	GND
4	GND
5	LCD PWRDNN
6	B (DIGITAL POT 10K)
7	W (DIGITAL POT 10K)
8	NC

P20 – LCD (LVDS) Connector

Pin No	Description
1	D3+
2	D3-
3	DPS
4	FRC
5	GND1
6	CK+
7	CK-
8	GND2
9	D2+
10	D2-
11	GND3
12	D1+
13	D1-
14	GND4
15	D0+
16	D0-
17	GND5
18	GND6
19	VCC1
20	VCC2

P21 – LCD (TFT 18bit)

Pin No	Pin Name
1	GND
2	VID_CLK_0
3	VID_HSYNC
4	VID_VSYNC
5	GND
6	VID_RED0
7	VID_RED1
8	VID_RED2
9	VID_RED3
10	VID_RED4
11	VID_RED5
12	GND
13	VID_GREEN0
14	VID_GREEN1
15	VID_GREEN2
16	VID_GREEN3
17	VID_GREEN4
18	VID_GREEN5
19	GND
20	VID_BLUE0
21	VID_BLUE1
22	VID_BLUE2

P21 – LCD (TFT 18bit) continued

Pin No	Pin Name
23	VID_BLUE3
24	VID_BLUE4
25	VID_BLUE5
26	GND
27	VID_BLANK#
28	+LCD_TFT
29	+LCD_TFT
30	SCANDIR1
31	SCANDIR2
32	NC
33	NC

P22 – LCD Touchscreen

Pin No	Pin Name
1	TS_XP
2	TS_YP
3	TS_XM
4	TS_YM
5	GND

P23 – Power Switch

(2 pin Header)

Pin No	Pin Name
1	SW1 TOGGLEN (PULSE, DEBOUCE)
2	GND

P24 – Hibernate Switch

(2 pin Header)

Pin No	Pin Name
1	SW2_TOGGLEN
1	GND

P27 – UART 1 Interface

Pin No	Pin Name
1	3.3 V
2	5 V
3	GND
4	GND
5	UART1_TXD
6	UART1_RXD
7	NC
8	NC

P28 – Audio

(10 pin Header)

Pin No	Pin Name
1	AUD_C_AUX_R
2	AUD_C_AUX_L
3	GND
4	GND
5	AUD_C_LOUT_R
6	AUD_C_LOUT_L
7	AUD_C_CD_GND
8	AUD_C_CD_GND
9	AUD_C_CD_INR
10	AUD_C_CD_INL

P29 – Micro-SD

Pin No	Pin Name
1	NC/DAT2
2	CPU_PATA_DACK#/CD_DAT3
3	CPU_PATA_IOW#/CMD
4	3.3v/Vcc
5	CPU_PATA_IOR#/CLOCK
6	GND/GND
7	CPU_PATA_IOCHRDY/DAT0
8	CPU_PATA_INTRQ/DAT1
9	NC/NC1
10	NC/NC2
11	NC/NC3
12	SD-CD#/CD_SW1
13	GND/CD_SW2
14	GND/GND1
15	GND/GND2
16	GND/GND3
17	GND/GND4

PWR-1 – ATX Power Connector

Pin No	Description
1	3.3VDC (FUSED - F2)
2	3.3VDC (FUSED - F2)
3	GND
4	5V, ONLY (WALL PS OR 4PIN CONNECTOR)
5	GND
6	5V, ONLY (WALL PS OR 4PIN CONNECTOR)
7	GND
8	POWER OK
9	5V STANDBY
10	12VDC
11	3.3VDC (FUSED - F2)
12	-12VDC
13	GND
14	POWER_ONN
15	GND
16	GND
17	GND
18	NC
19	5VDC
20	5VDC

PWR-2 – 5V Power Connector

Pin No	Pin Name
1	5V
2	GND
3	Pwer_Basrrel 6
4	5V

J05 – SATA

Pin No	Pin Name
1	GND
2	CPU SATA TXP
3	CPU SATA TXN
4	GND
5	CPU SATA RXN
6	CPU SATA RXP
7	GND
8	GND
9	GND

Glossary

Below is a list of common terms and acronyms you may find incorporated in this manual.

AC97 ..... Audio Codec driver
ATX ..... Advanced Technology Extended (mother board form factor)
AXE ..... 32-bit RISC Audio Acceleration Engine
BDLC ..... Byte Data Link Controller
CAN ..... Controller Area Network
COP ..... Debug Port
CPLD ..... Complex Programmable Logic Device
CPU ..... Central Processor Unit
DDR ..... Double Data Rate (RAM)
DMA ..... Direct Memory Access
DSP ..... Digital Signal Processor
DVI ..... Digital Video Interface/Input
EMB ..... External Memory Bus
FEC ..... Fast Ethernet Controller
GIGE ..... Gigabit Ethernet
GMII ..... Gigabit Media Independent Interface
GPIO ..... General Purpose Input/Output
GPT ..... General Purpose Timers
HDD ..... Hard Disk Drive
I^2C (IIC) ..... Inter-Integrated Circuit
J1850 ..... CAN Protocol (Ford, GM, Chrysler)
IPIC ..... Integrated Programmable Interrupt
JTAG ..... Test Port per IEEE 1149
LCD ..... Liquid Crystal Display
LPC ..... LocalPlus Bus
LVDS ..... Low Voltage Differential Signaling
MBX ..... Power VR® MBX Lite IP (Intergrated Graphics Engine by Imagination Technologies)
MDIO ..... Management Data Input/Output
Mini-ITX ..... Low Power Motherboard Standard (17cm x 17cm form factor)
NFC ..... NAND Flash Controller
OTG ..... On The Go (USB)
PATA ..... Parallel AT Attachment
PCI ..... Peripheral Component Interconnect
PMC ..... Power Management Control
PSC ..... Programmable Serial Channel
RAM ..... Random Access Memory
RGMII ..... Reduced Gigabit Media Independent Interface
RMII ..... Reduced Media Independent Interface
RTC ..... Real Time Clock
SAP ..... System Access Port
SATA ..... Serial Advanced Technology Attachment
SPDIF ..... Sony-Philips Digital-audio Interface Format
TLM ..... Tap Linking Module
TPM ..... Test Port to Magenta Module
TSEC ..... Triple Speed Ethernet Controller
USB ..... Universal Serial Bus
VBAT ..... Battery Voltage
WDT ..... Watchdog Timer
WP ..... Write Protect